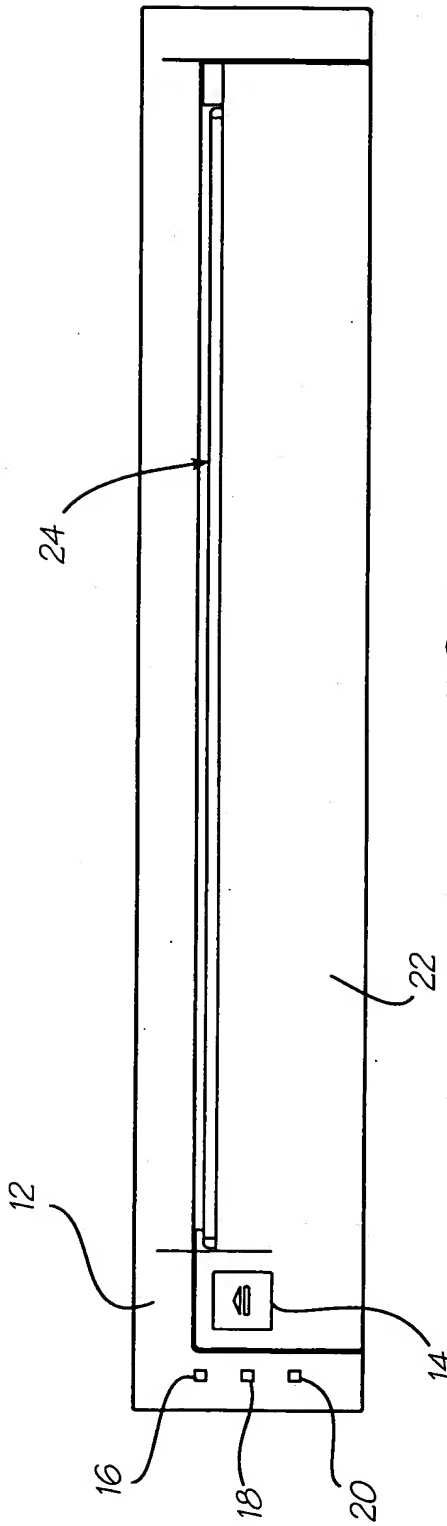


FIG. 1

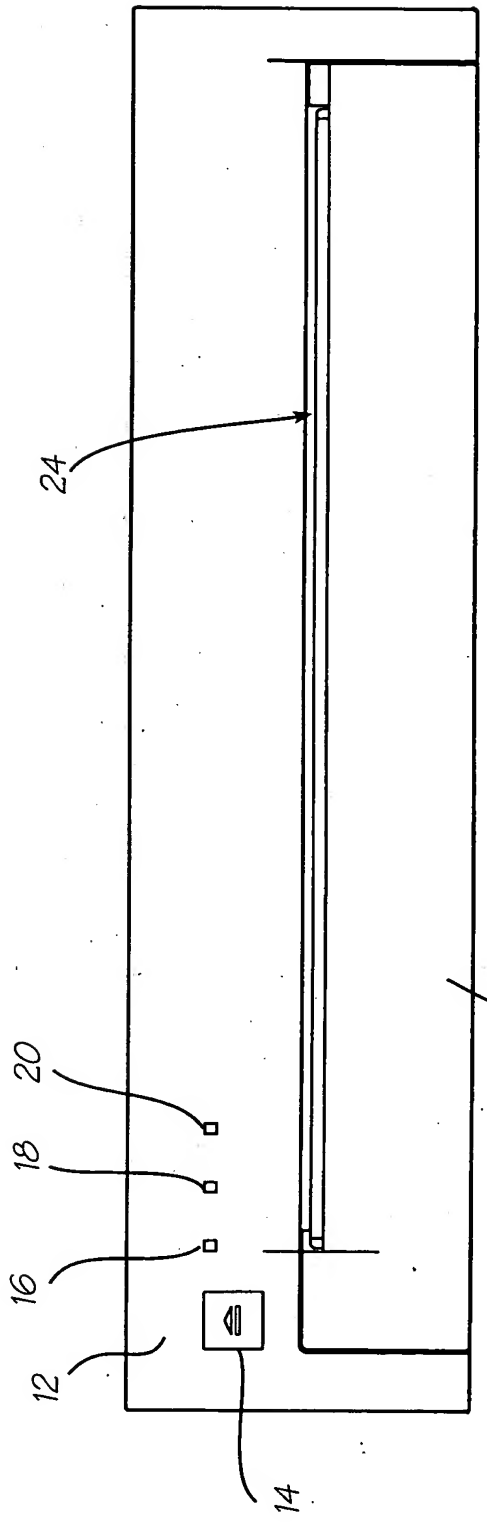


FIG. 2

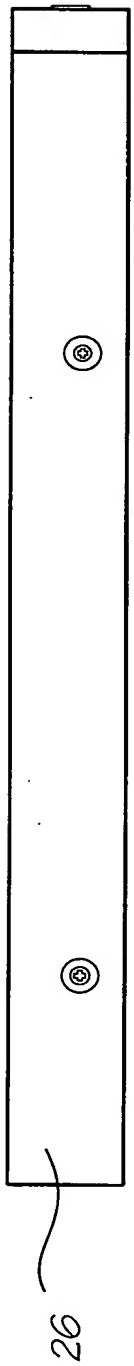


FIG. 3

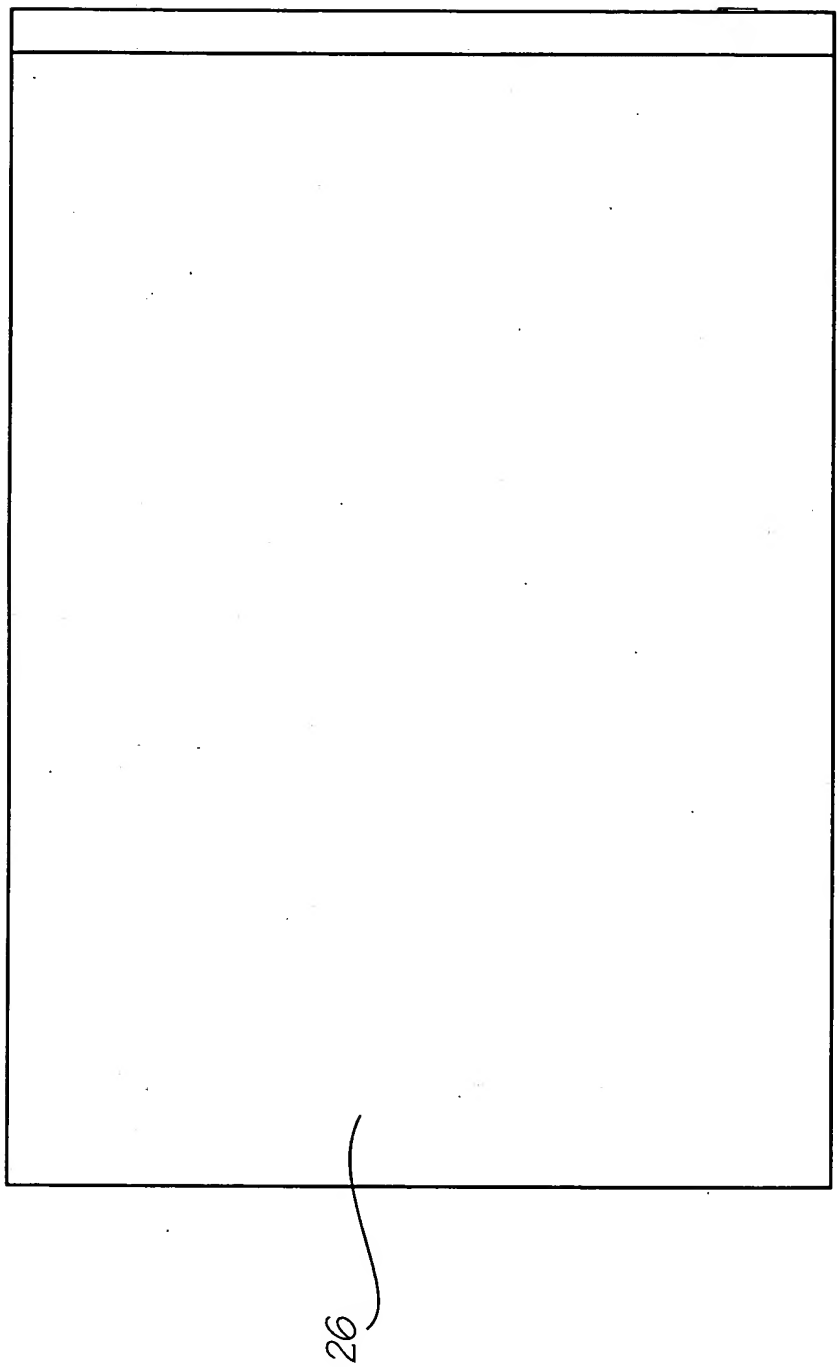


FIG. 4

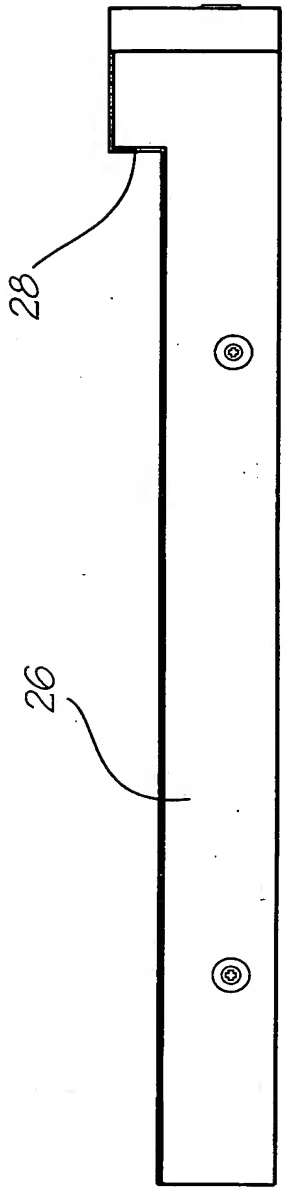


FIG. 5

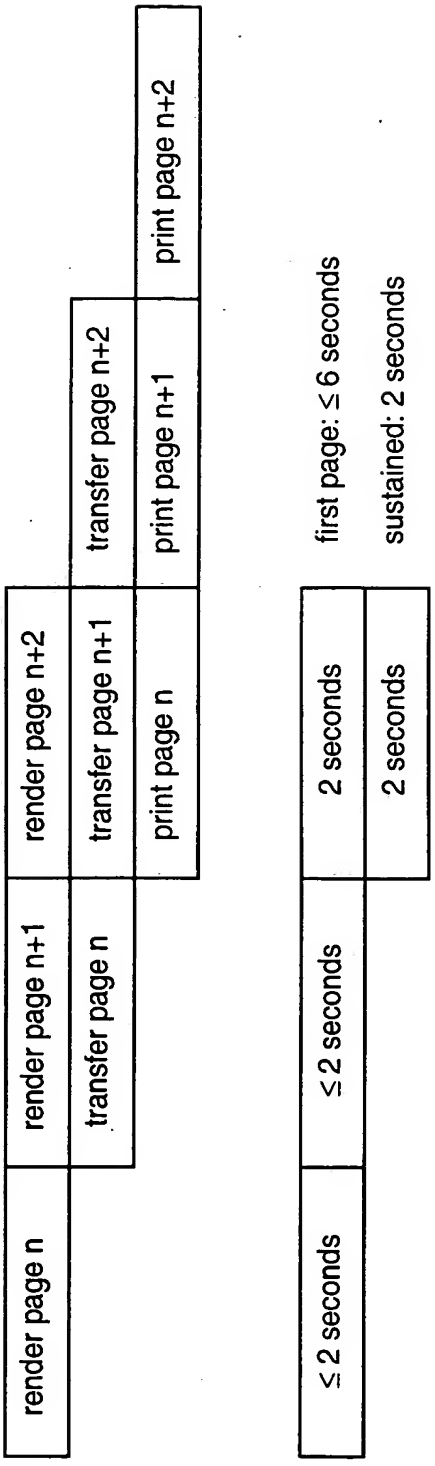

render page n
render page n+1
transfer page n
render page n+2
transfer page n+1
print page n
transfer page n+2
print page n+1
print page n+2
≤ 2 seconds
≤ 2 seconds
2 seconds
2 seconds
first page: ≤ 6 seconds
sustained: 2 seconds

FIG. 6

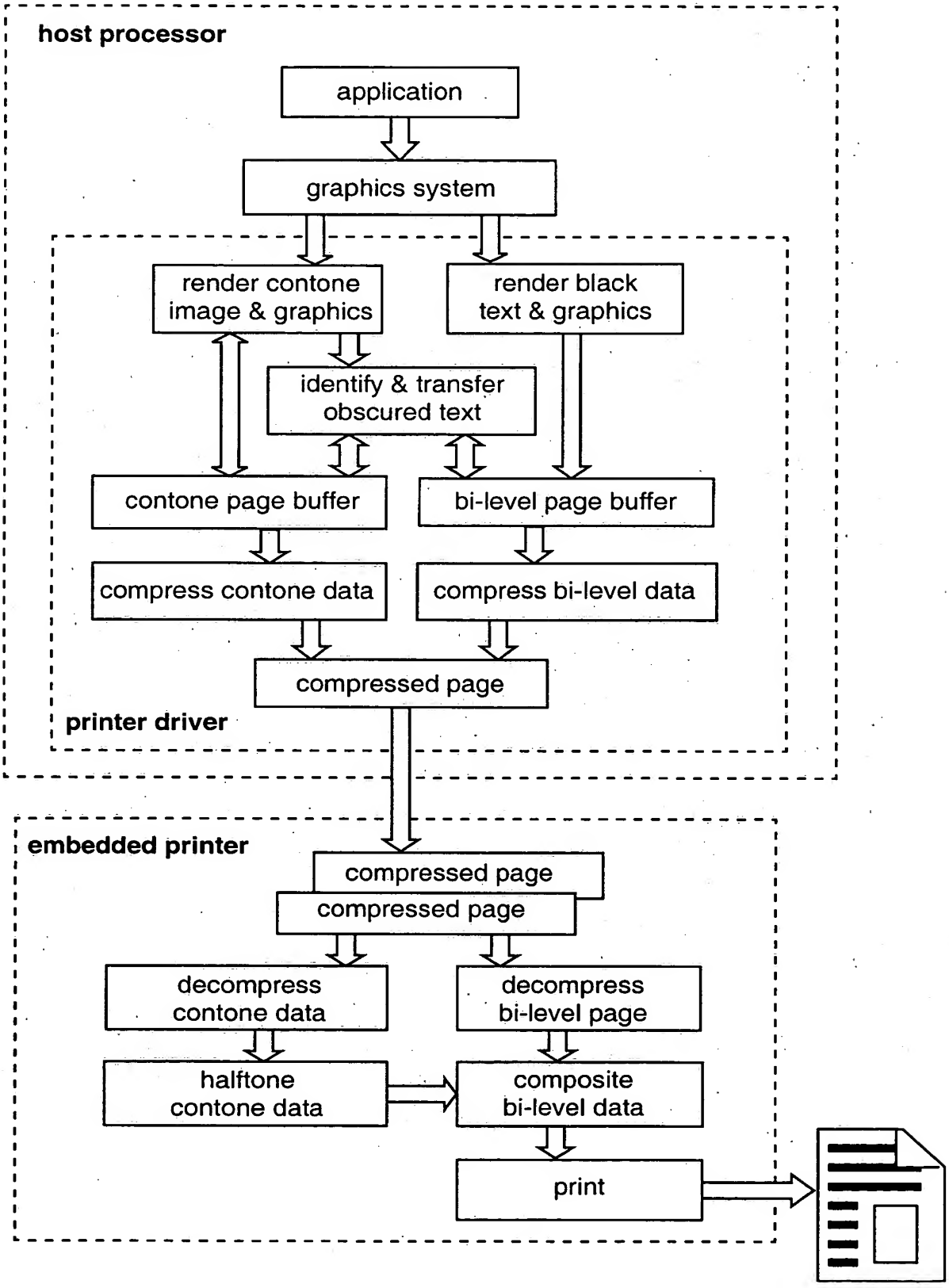

host processor
application
graphics system
render contone image & graphics
render black text & graphics
identify & transfer obscured text
contone page buffer
bi-level page buffer
compress contone data
compress bi-level data
compressed page
printer driver
embedded printer
compressed page
compressed page
decompress contone data
decompress bi-level page
halftone contone data
composite bi-level data
print

FIG. 7

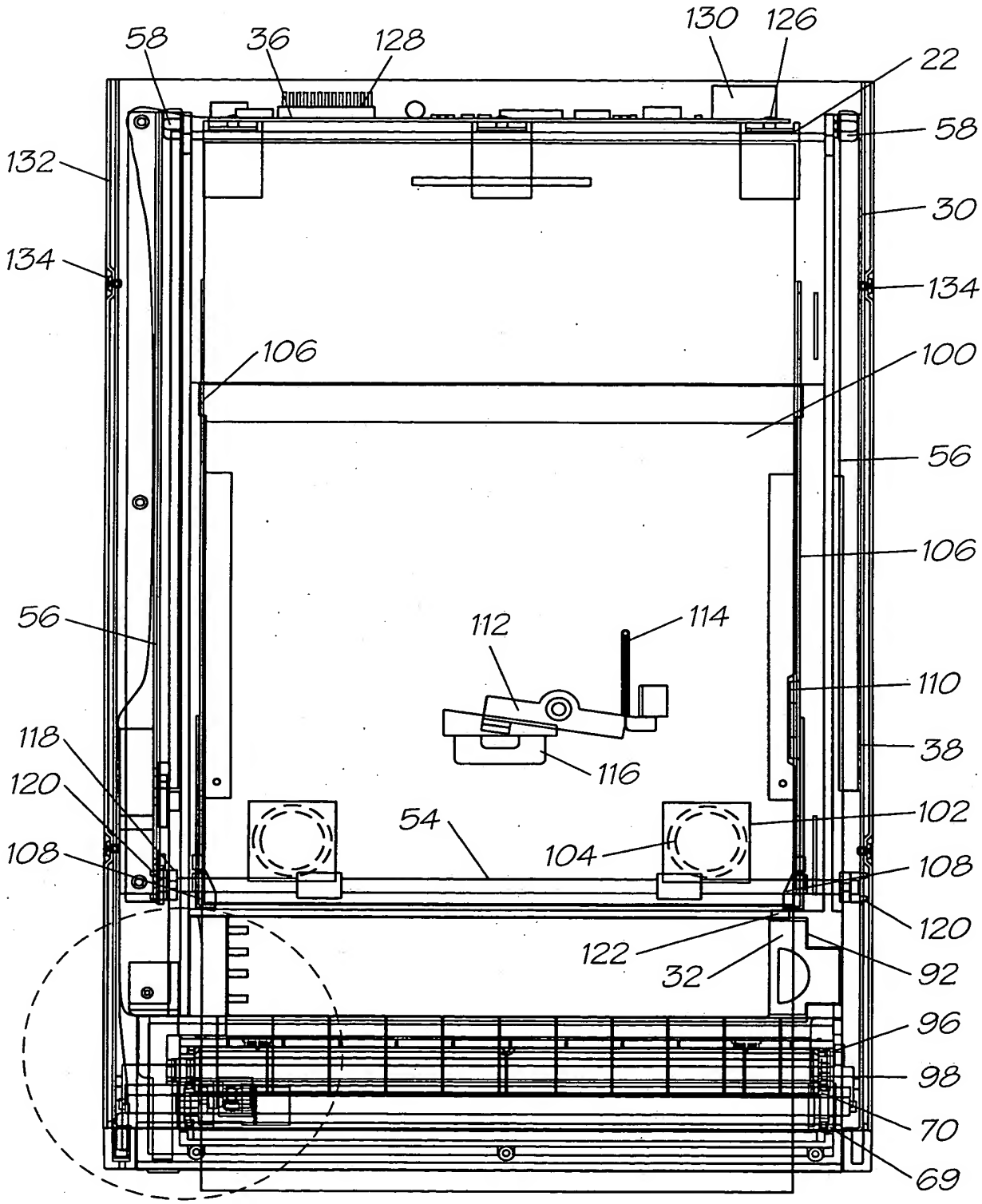

58
36
128
130
126
22
132
58
30
134
134
106
100
56
106
56
112
114
110
118
116
38
120
54
102
108
104
108
120
122
92
32
96
98
70
69

FIG. 8

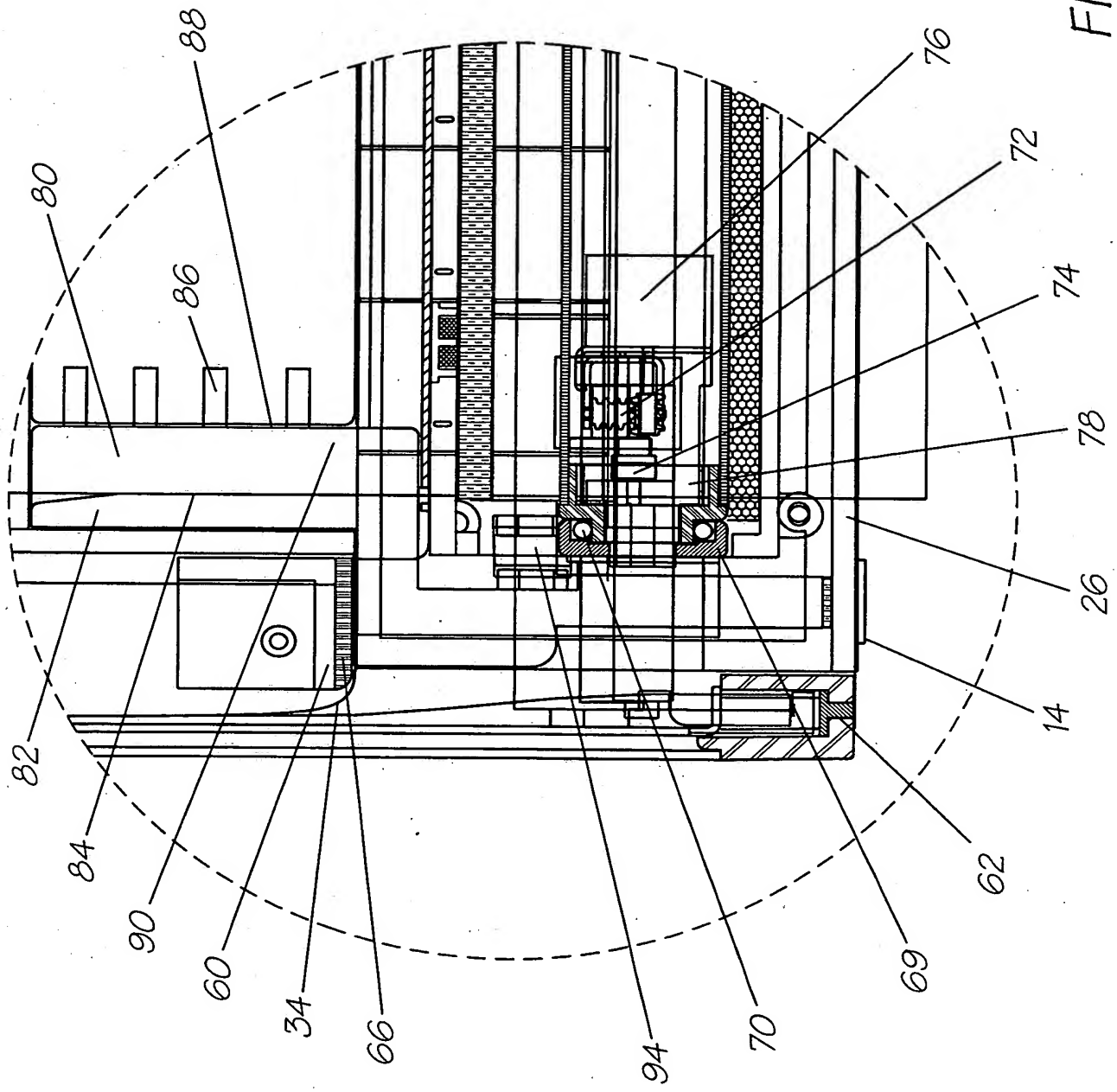


FIG. 8A

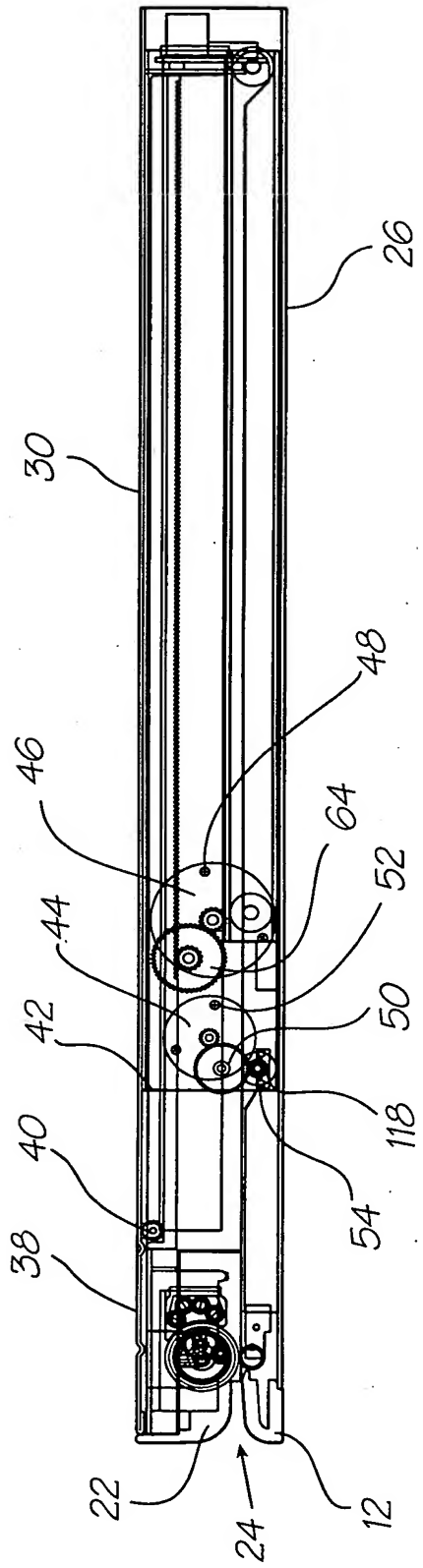

26
30
48
46
64
52
44
50
42
118
40
54
38
22
24
12

FIG. 9

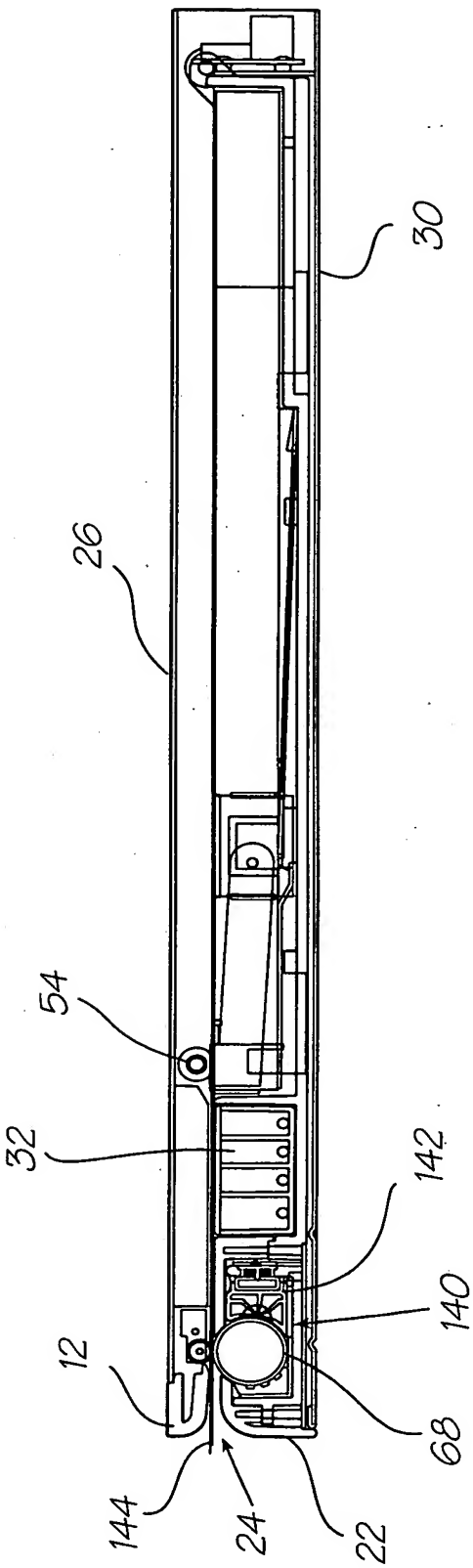

30
26
54
32
142
140
12
68
144
24
22

FIG. 10

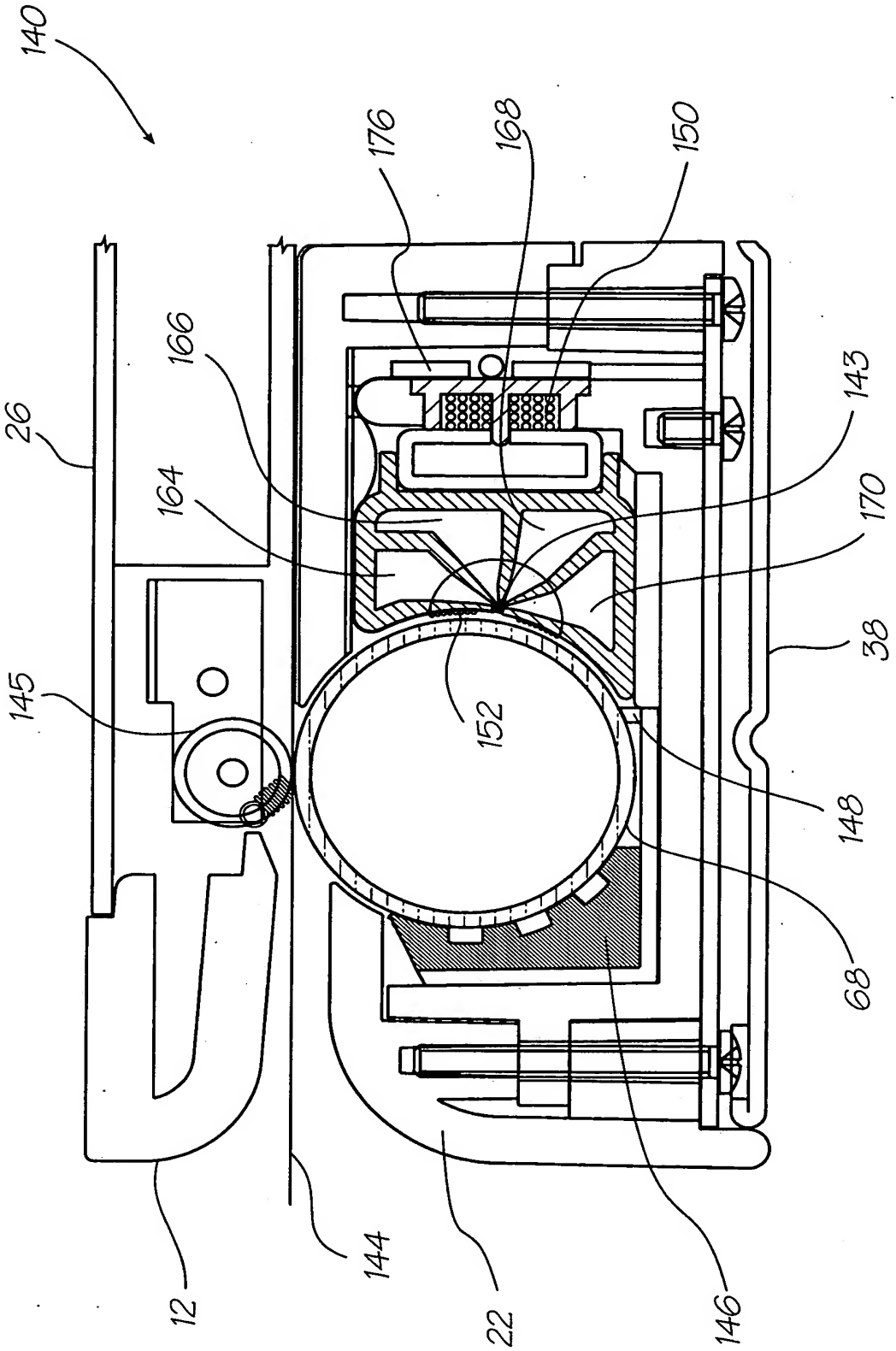


FIG. 11

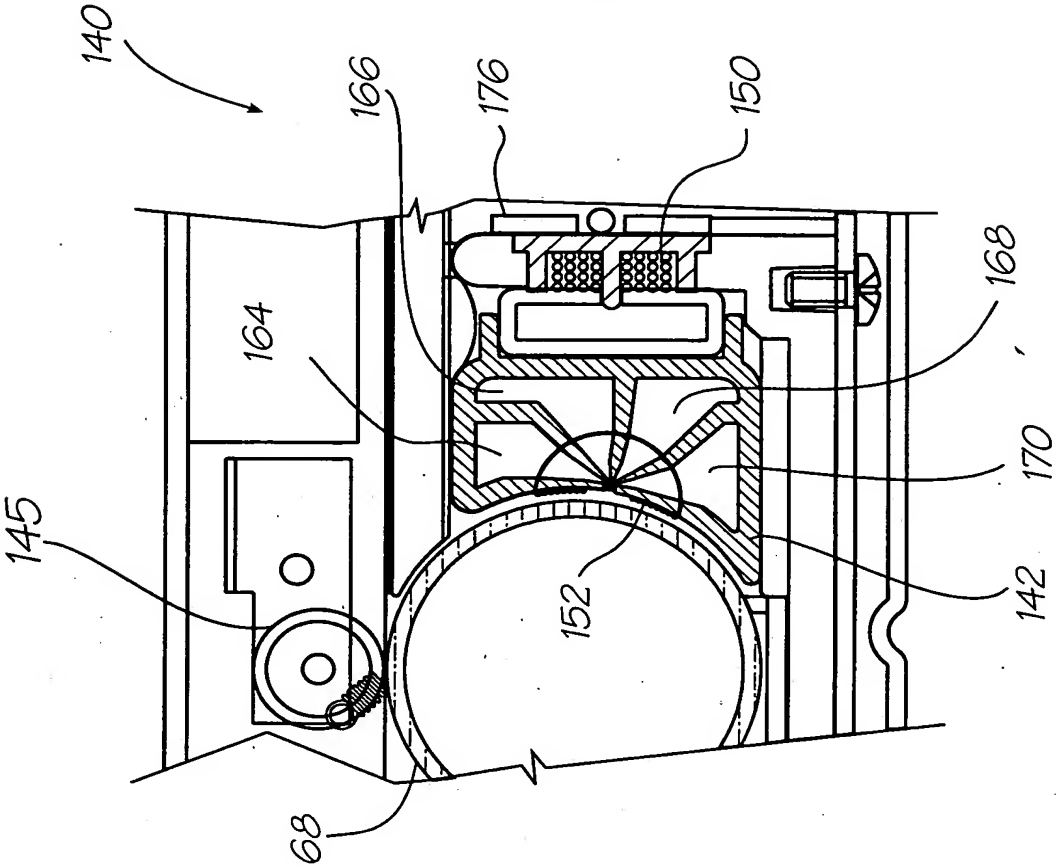


FIG. 12B

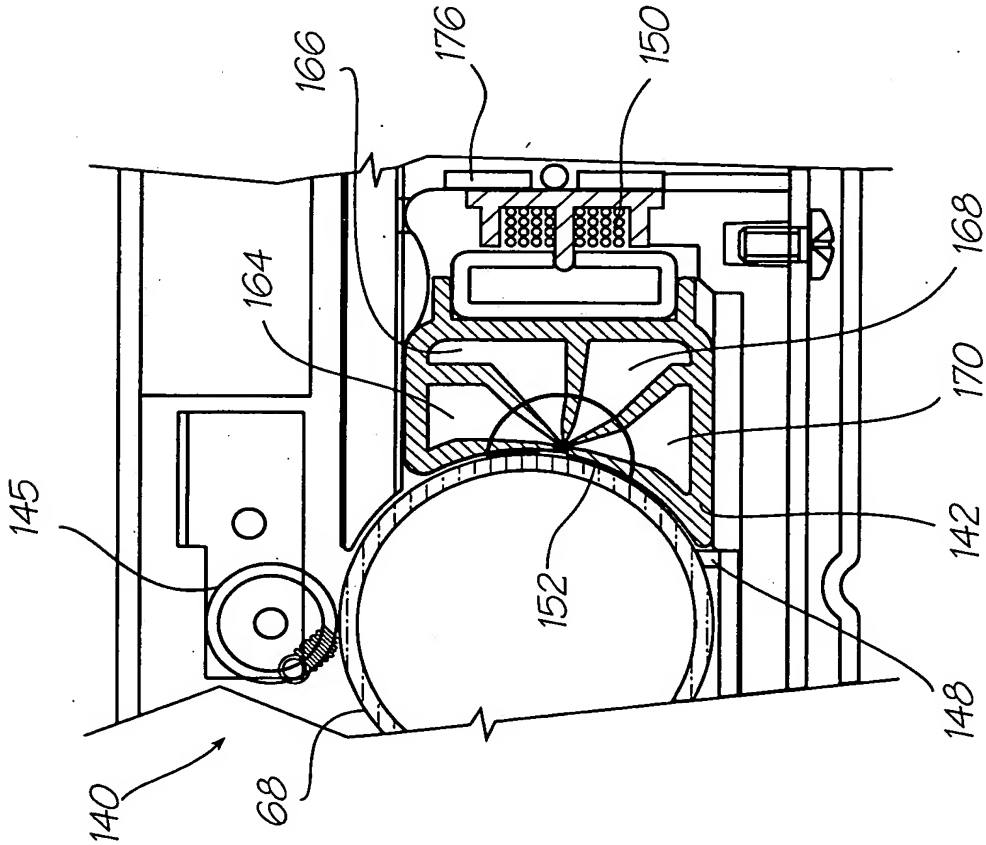


FIG. 12A

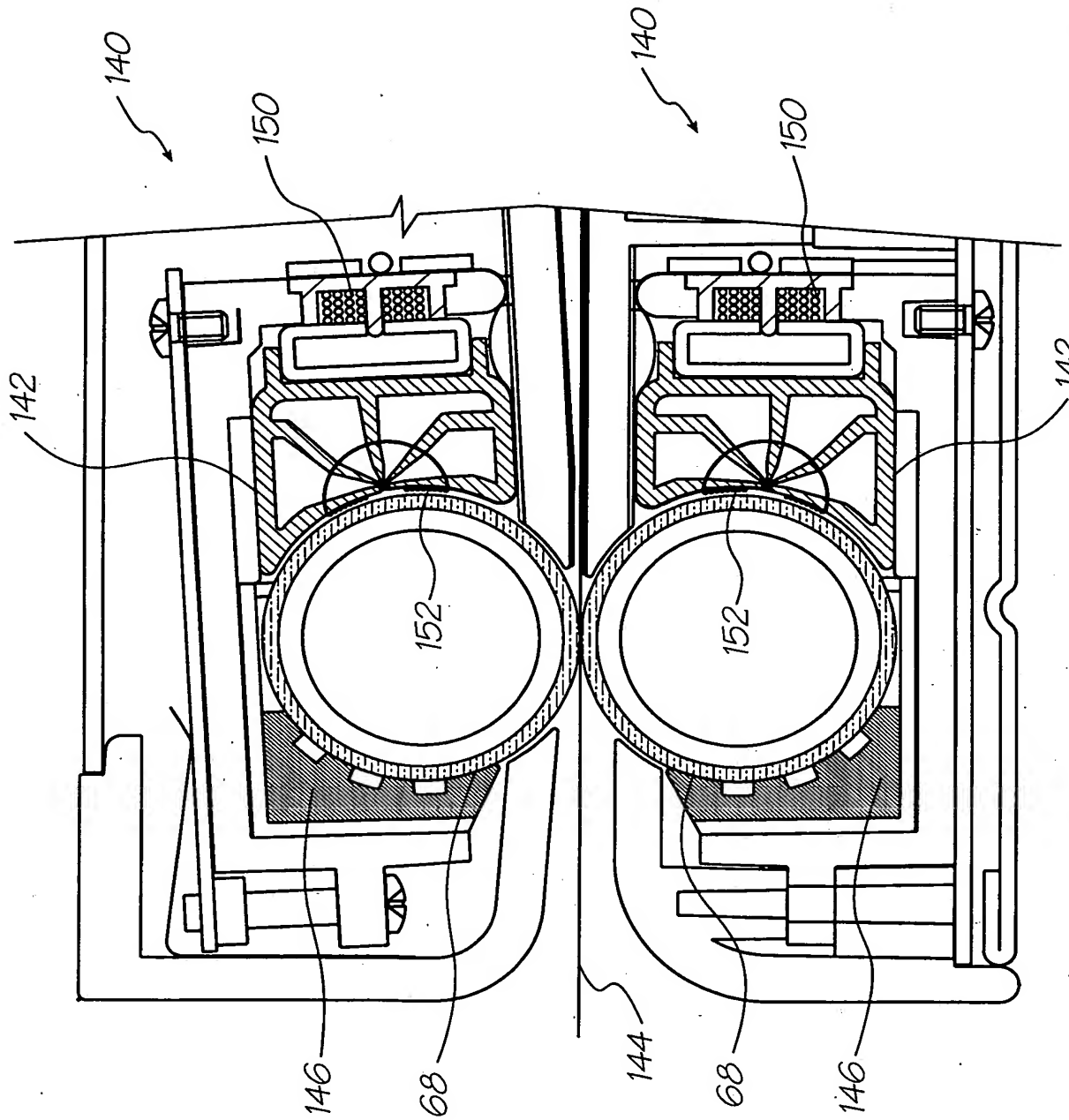


FIG. 13

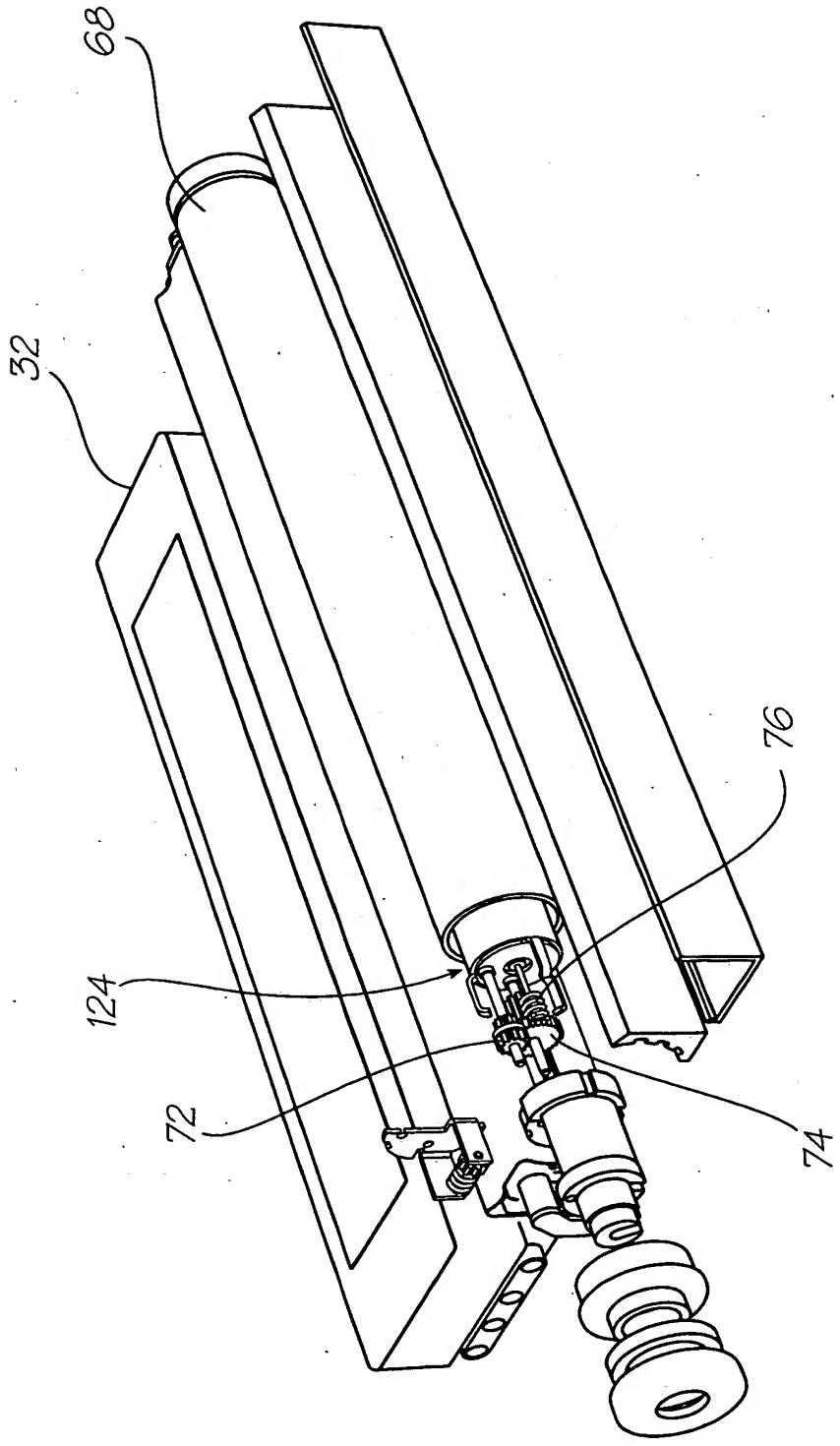


FIG. 14

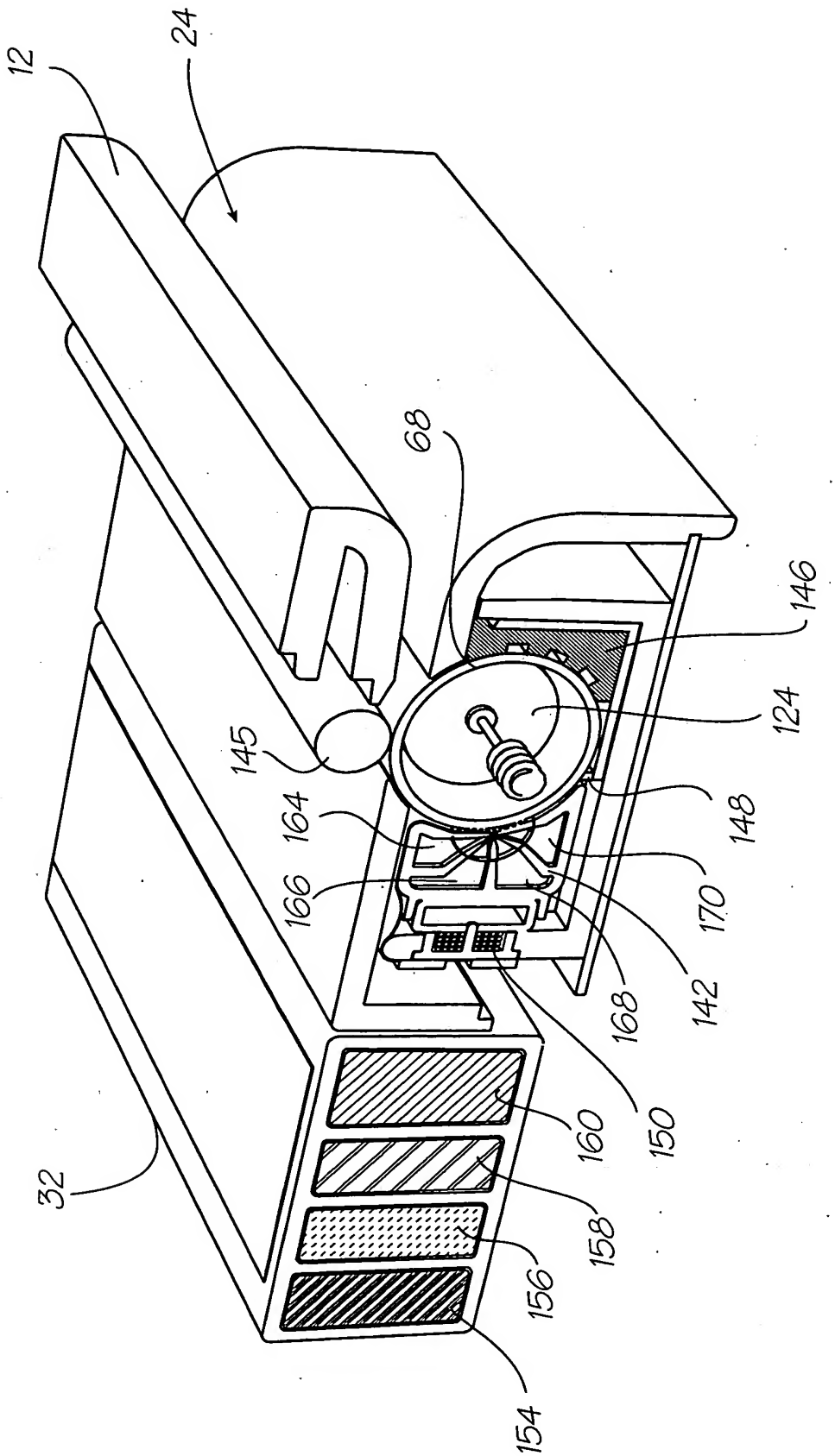

12
24
68
146
124
145
164
148
166
170
142
168
150
160
158
156
154
32

FIG. 15

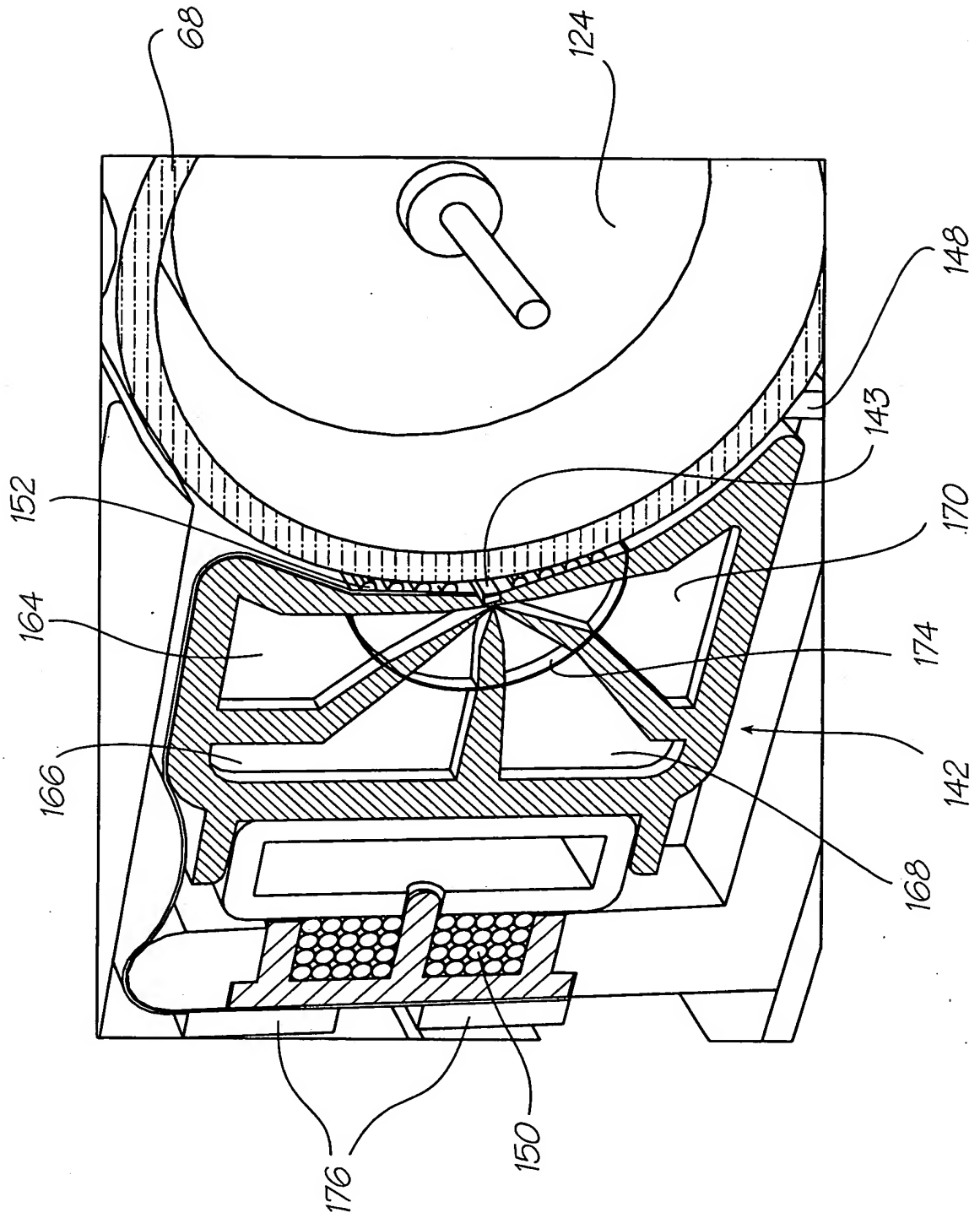
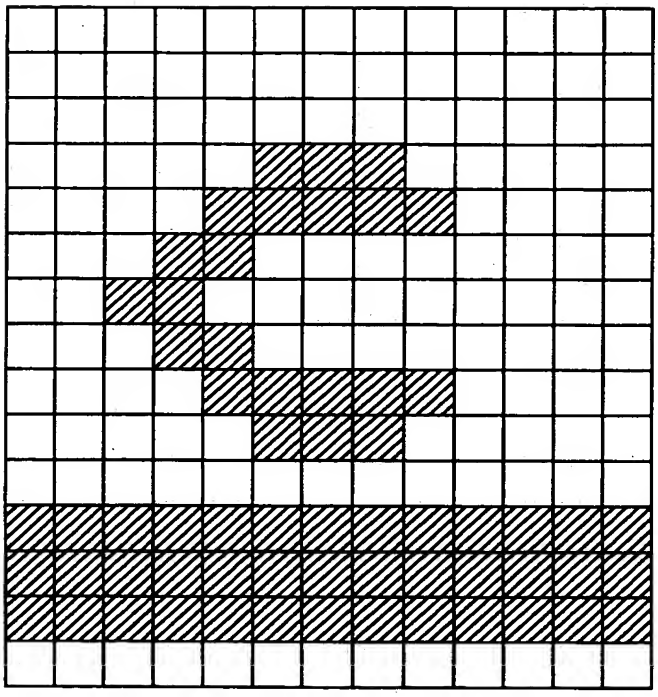


FIG. 16



Δ0
Δ0
Δ0
create 5, create 3, Δ0
Δ−1, Δ+1, Δ0
Δ−1, create 2, kill, Δ0
Δ−1, Δ−1, Δ0
Δ+1, Δ+1, Δ0
Δ+1, kill, create 5, Δ0
Δ+1, Δ−1, Δ0
kill, kill, Δ0
create 0, kill, create 13
Δ0, Δ0
Δ0, Δ0
kill, kill, create 13, EOP

FIG. 17

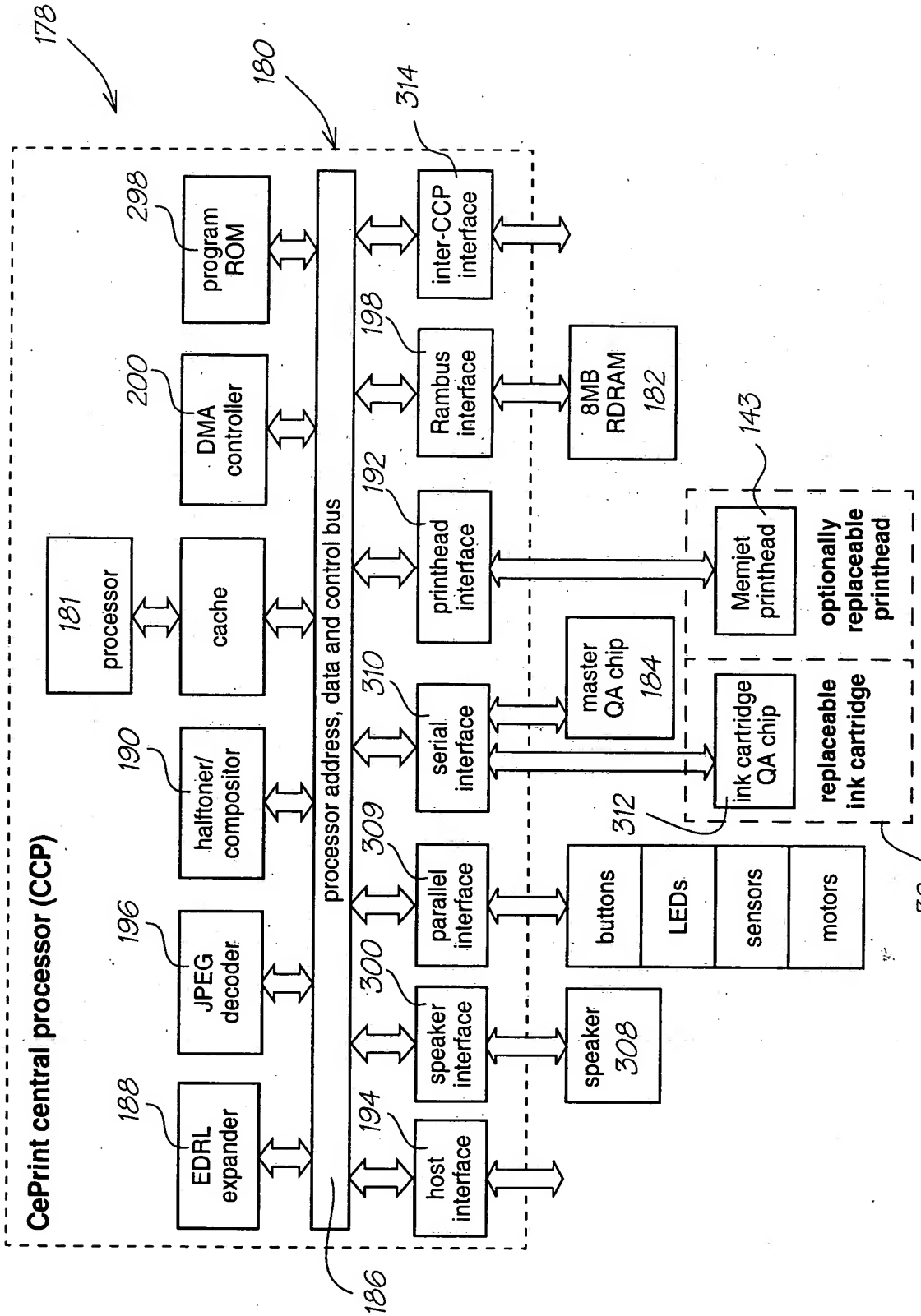

178
180
314
298
program ROM
inter-CCP interface
200
DMA controller
198
Rambus interface
8MB RDRAM 182
181 processor
cache
192
printhead interface
143
Memjet printhead
optionally replaceable printhead
CePrint central processor (CCP)
processor address, data and control bus
190
halftoner/ compositor
310
serial interface
master QA chip 184
ink cartridge QA chip
replaceable ink cartridge
196
JPEG decoder
309
parallel interface
312
buttons
LEDs
sensors
motors
32
188
EDRL expander
300
speaker interface
speaker 308
194
host interface
186

FIG. 18

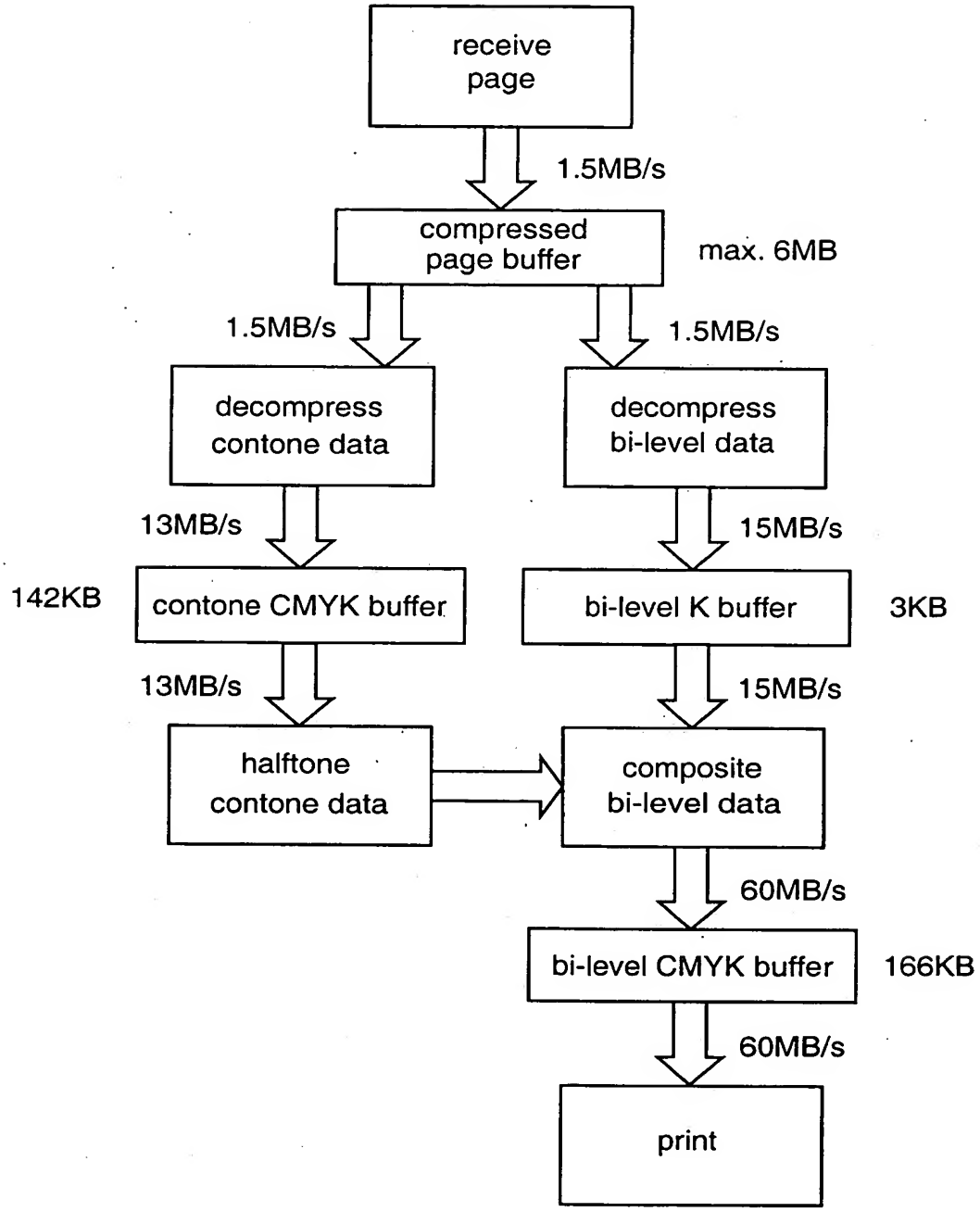

receive page
1.5MB/s
compressed page buffer
max. 6MB
1.5MB/s
1.5MB/s
decompress contone data
decompress bi-level data
13MB/s
15MB/s
142KB
contone CMYK buffer
bi-level K buffer
3KB
13MB/s
15MB/s
halftone contone data
composite bi-level data
60MB/s
bi-level CMYK buffer
166KB
60MB/s
print

FIG. 19

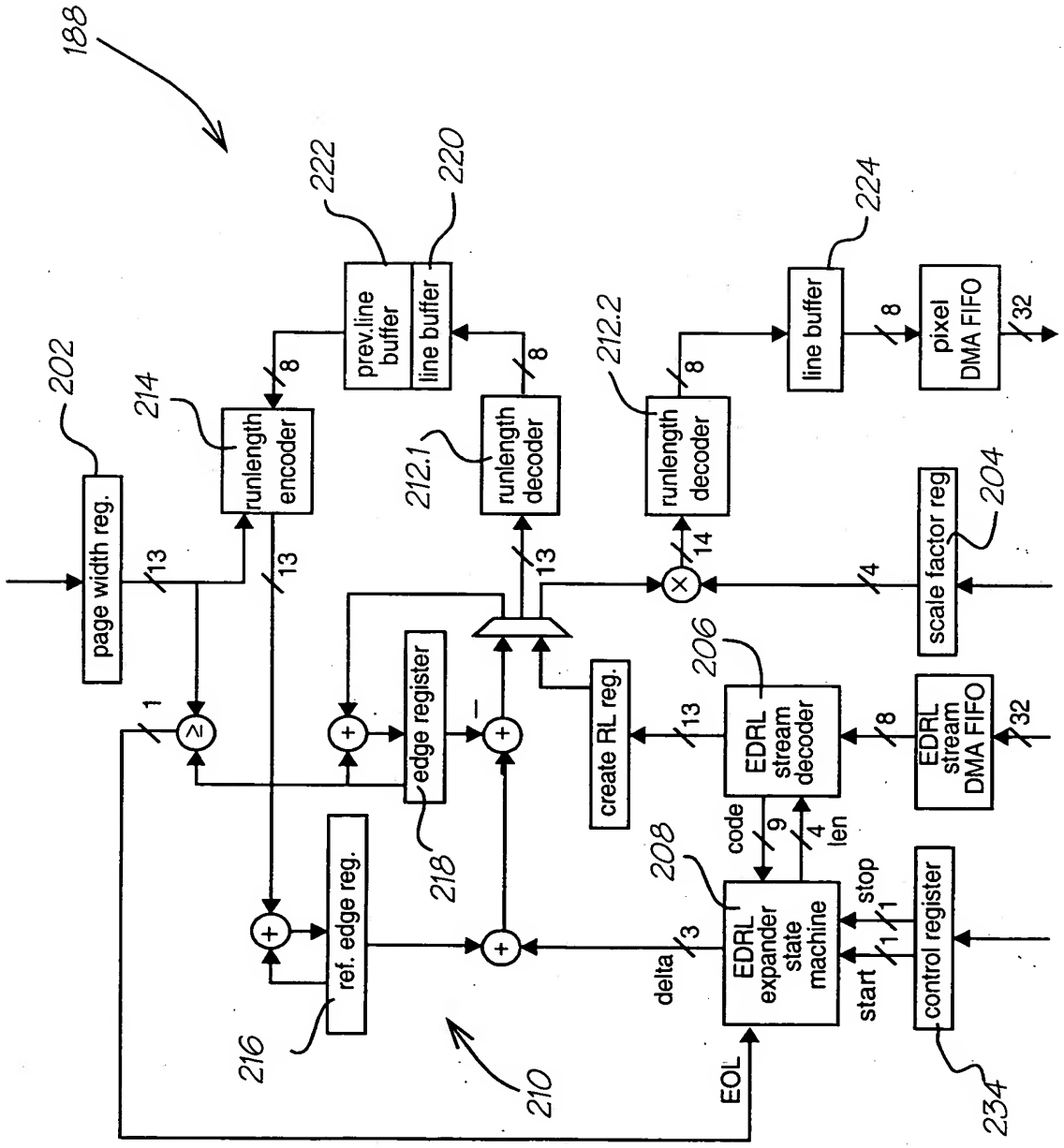

188
202
page width reg.
214
runlength encoder
222
prev.line buffer
220
line buffer
212.1
runlength decoder
212.2
runlength decoder
224
line buffer
pixel DMA FIFO
204
scale factor reg
206
EDRL stream decoder
EDRL stream DMA FIFO
create RL reg.
edge register
218
ref. edge reg.
216
208
EDRL expander state machine
code
len
stop
start
control register
delta
EOL
210
234

FIG. 20

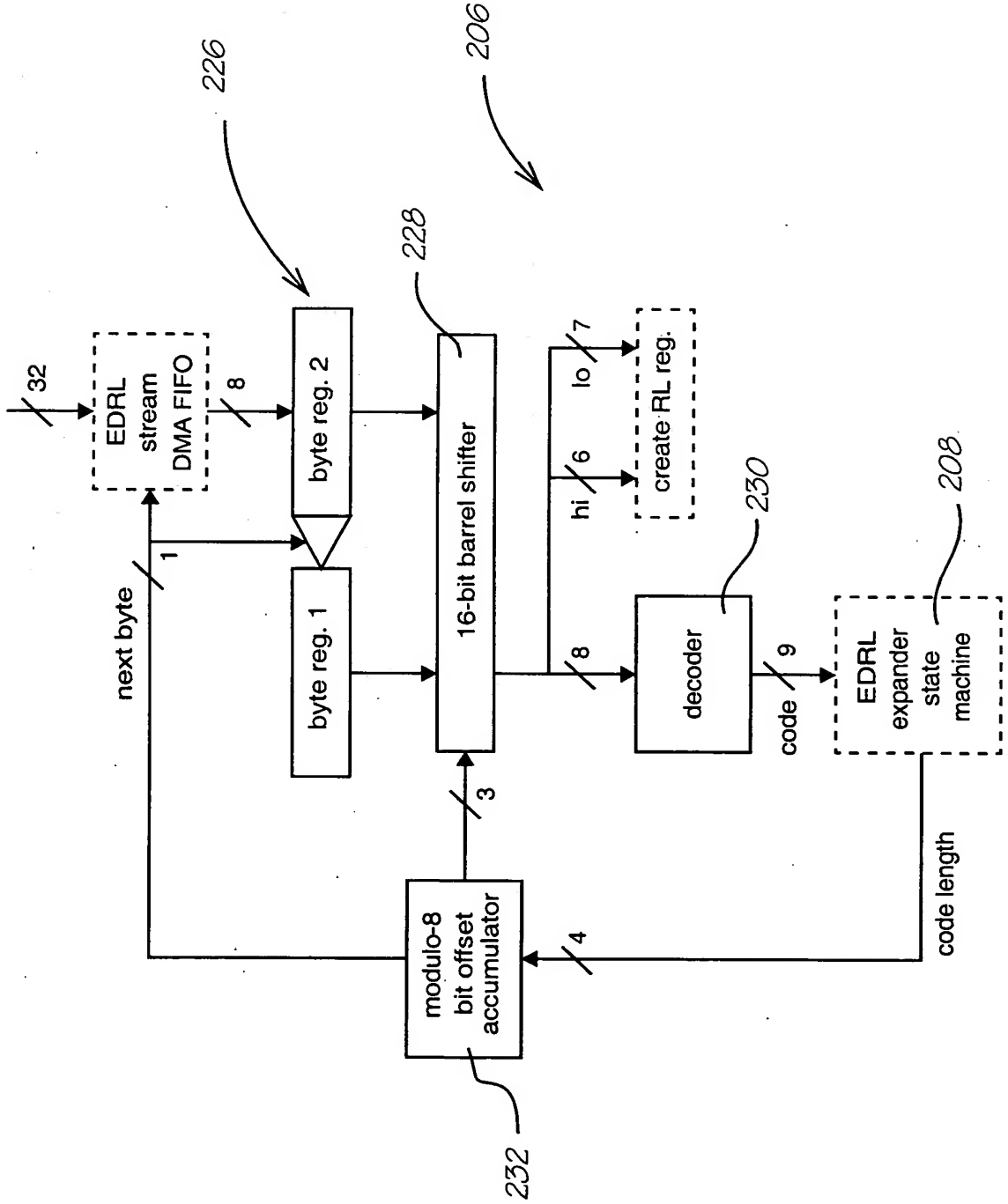

206
226
228
32
EDRL stream DMA FIFO
8
byte reg. 2
byte reg. 1
16-bit barrel shifter
7
lo
6
hi
create RL reg.
next byte
1
8
decoder
230
9
code
EDRL expander state machine
208
3
modulo-8 bit offset accumulator
4
code length
232

FIG. 21

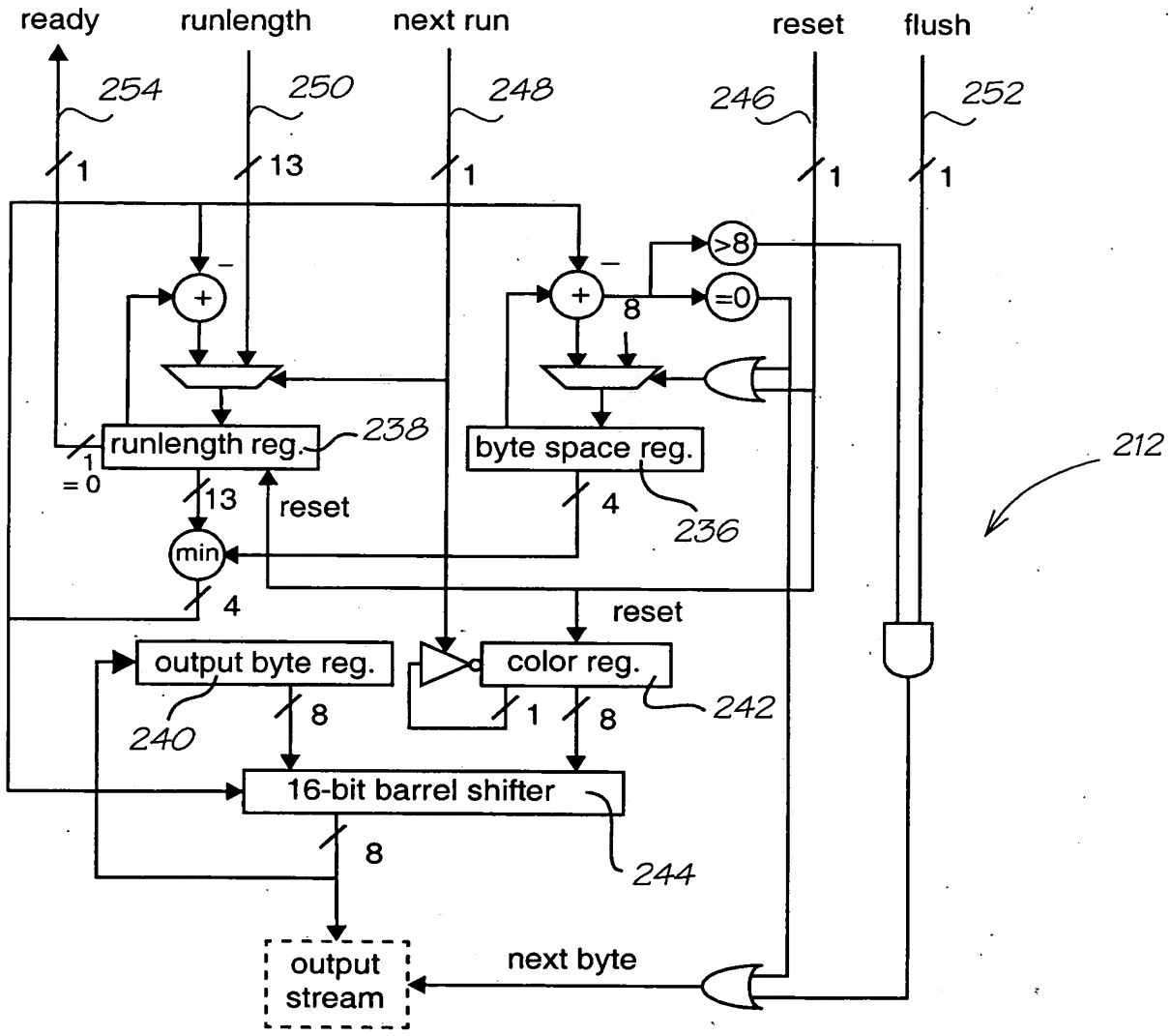

ready
runlength
next run
reset
flush
254
250
248
246
252
1
13
1
1
1
+
−
+
−
>8
=0
8
runlength reg.
238
byte space reg.
212
1
= 0
13
reset
4
236
min
4
reset
output byte reg.
color reg.
240
8
1
8
242
16-bit barrel shifter
8
244
output
stream
next byte

FIG. 22

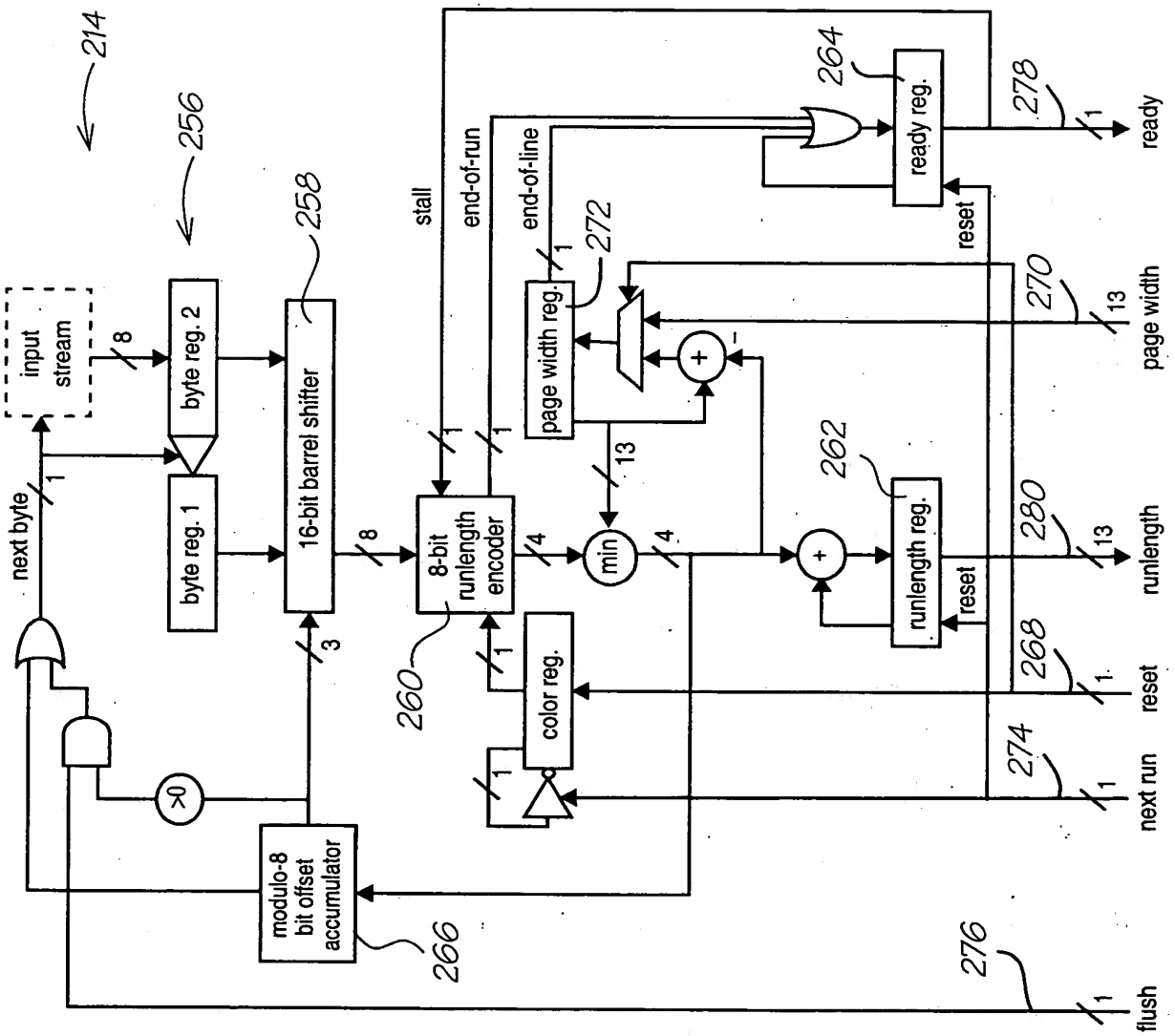

214
256
258
input stream
8
byte reg. 2
byte reg. 1
16-bit barrel shifter
next byte
1
8
3
>0
modulo-8 bit offset accumulator
266
stall
end-of-run
end-of-line
1
1
1
8-bit runlength encoder
260
4
min
4
color reg.
1
1
page width reg.
272
13
13
-
+
270
page width
262
+
runlength reg.
reset
280
13
runlength
264
ready reg.
reset
278
1
ready
268
1
reset
274
1
next run
276
1
flush

FIG. 23

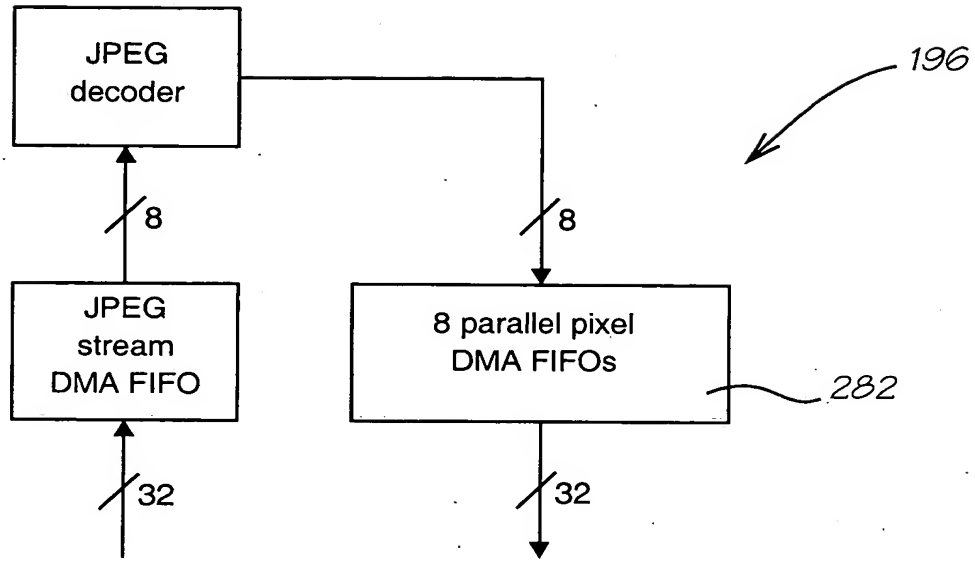

JPEG
decoder
196
8
8
JPEG
stream
DMA FIFO
8 parallel pixel
DMA FIFOs
282
32
32

FIG. 24

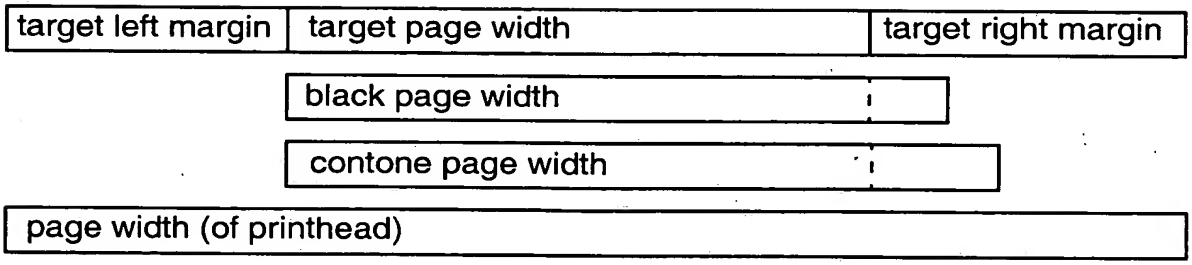

target left margin
target page width
target right margin
black page width
contone page width
page width (of printhead)

FIG. 26

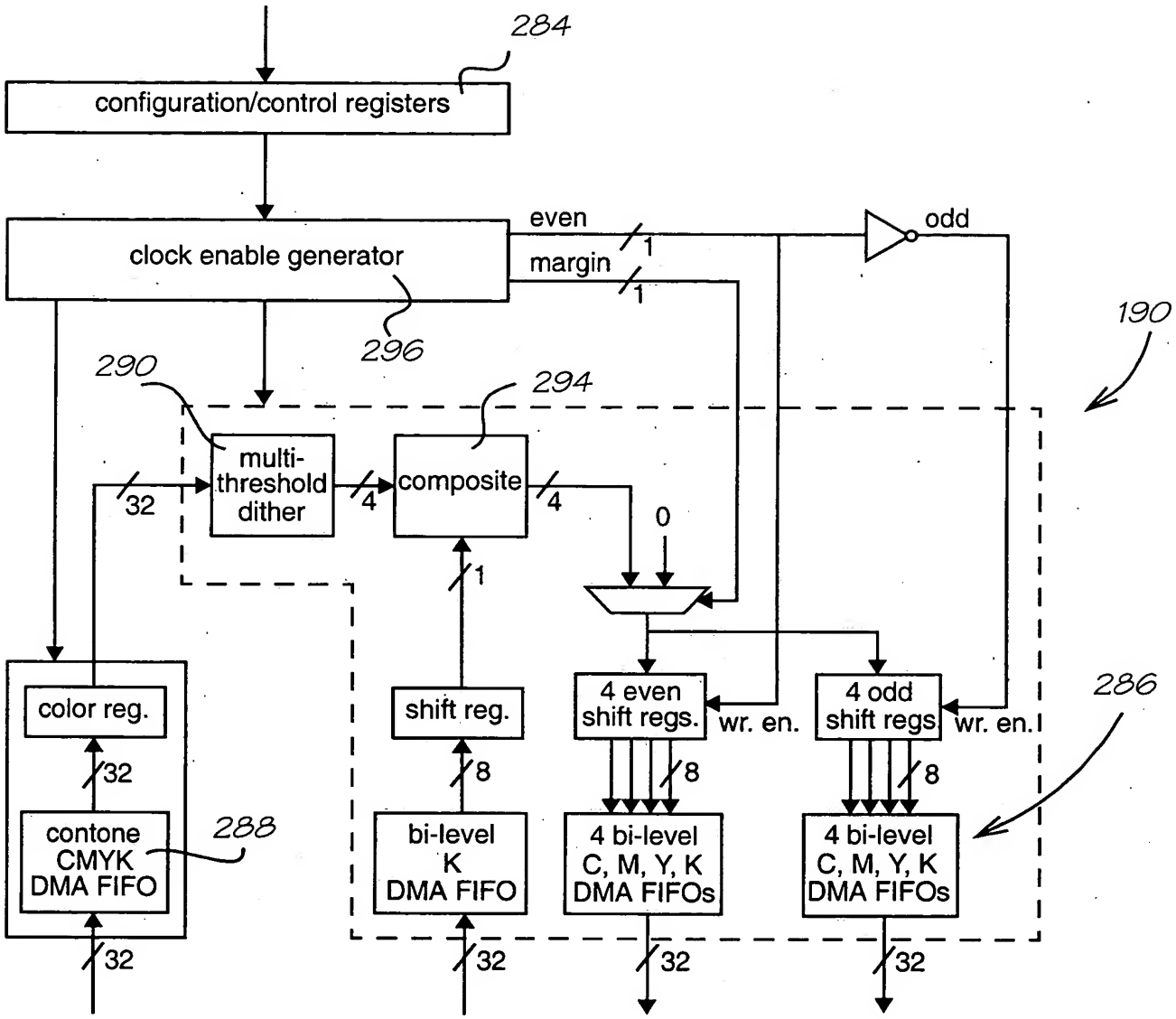

284
configuration/control registers
clock enable generator
296
even
margin
1
1
odd
190
290
294
multi-threshold dither
32
4
composite
4
0
1
color reg.
32
contone CMYK DMA FIFO
288
32
shift reg.
8
bi-level K DMA FIFO
32
4 even shift regs.
wr. en.
8
4 bi-level C, M, Y, K DMA FIFOs
32
4 odd shift regs
wr. en.
8
4 bi-level C, M, Y, K DMA FIFOs
32
286

FIG. 25

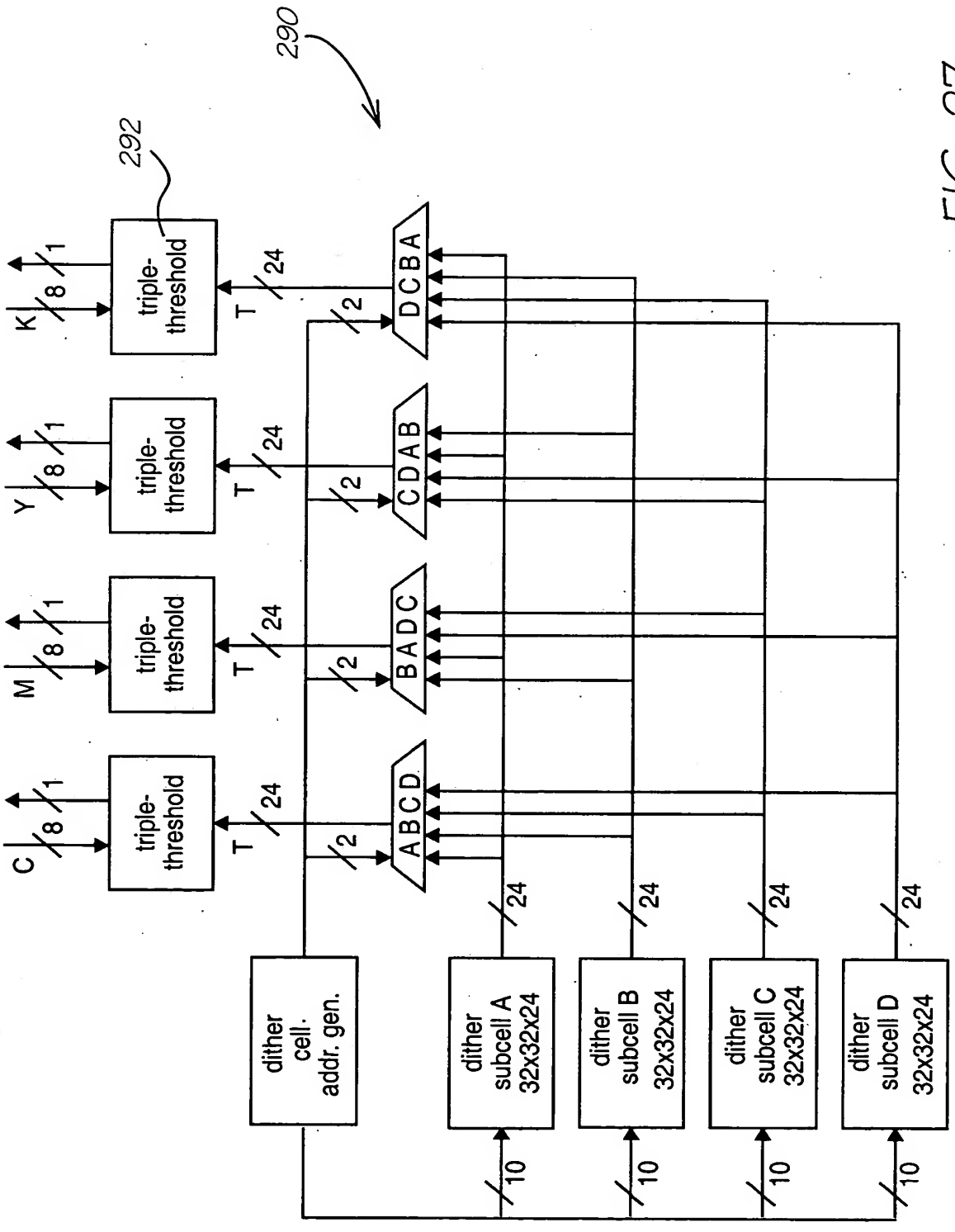

290
292
K
Y
M
C
8
1
triple-threshold
T
24
2
DCBA
CDAB
BADC
ABCD
dither cell addr. gen.
dither subcell A 32x32x24
dither subcell B 32x32x24
dither subcell C 32x32x24
dither subcell D 32x32x24
10

FIG. 27

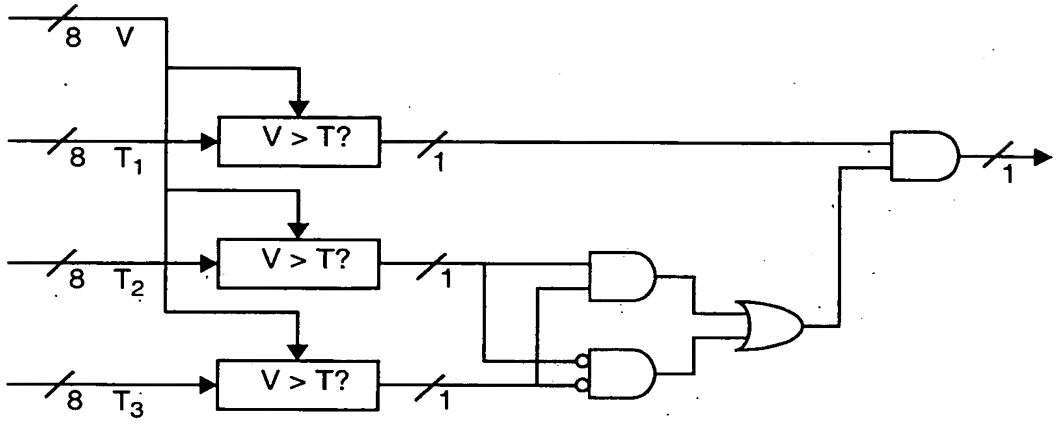

8 V
8 T1
8 T2
8 T3
V > T?
V > T?
V > T?
1
1
1
1

FIG. 28

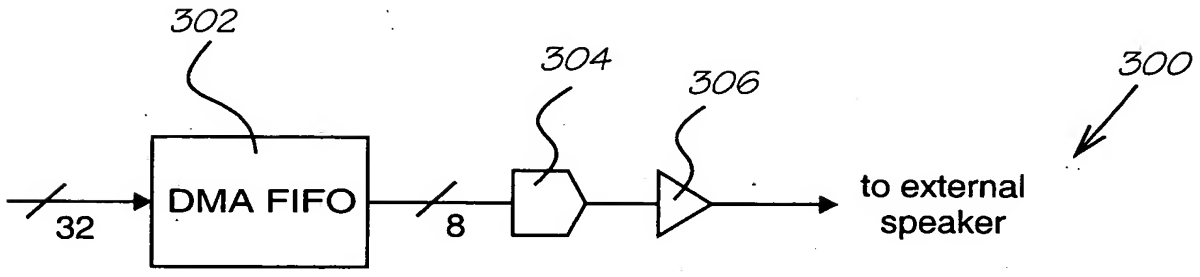

302
304
306
300
32
DMA FIFO
8
to external
speaker

FIG. 29

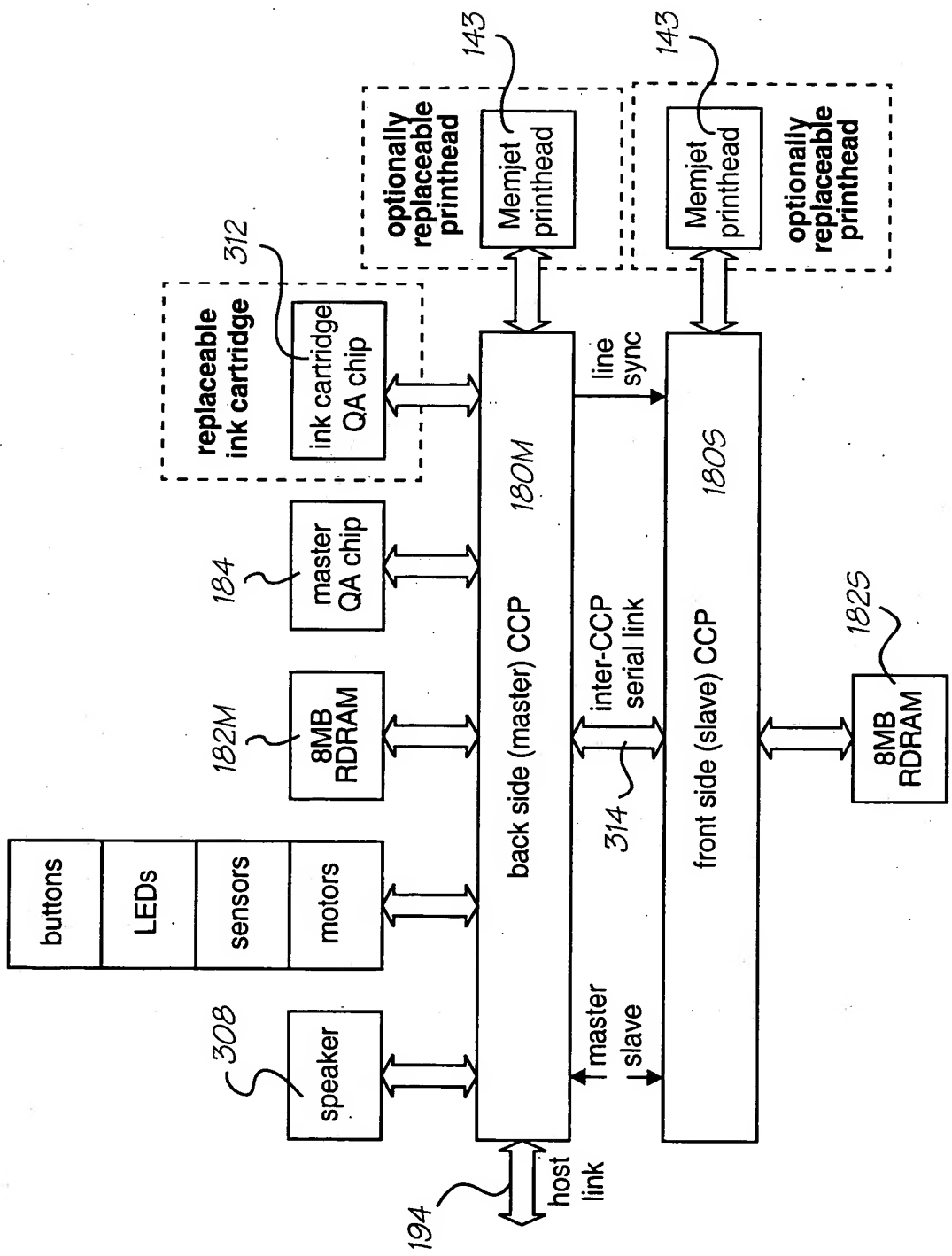

buttons
LEDs
sensors
motors
speaker
308
182M
8MB RDRAM
184
master QA chip
replaceable ink cartridge
312
ink cartridge QA chip
back side (master) CCP
180M
optionally replaceable printhead
143
Memjet printhead
line sync
inter-CCP serial link
314
master
slave
front side (slave) CCP
180S
optionally replaceable printhead
143
Memjet printhead
182S
8MB RDRAM
host link
194

FIG. 30

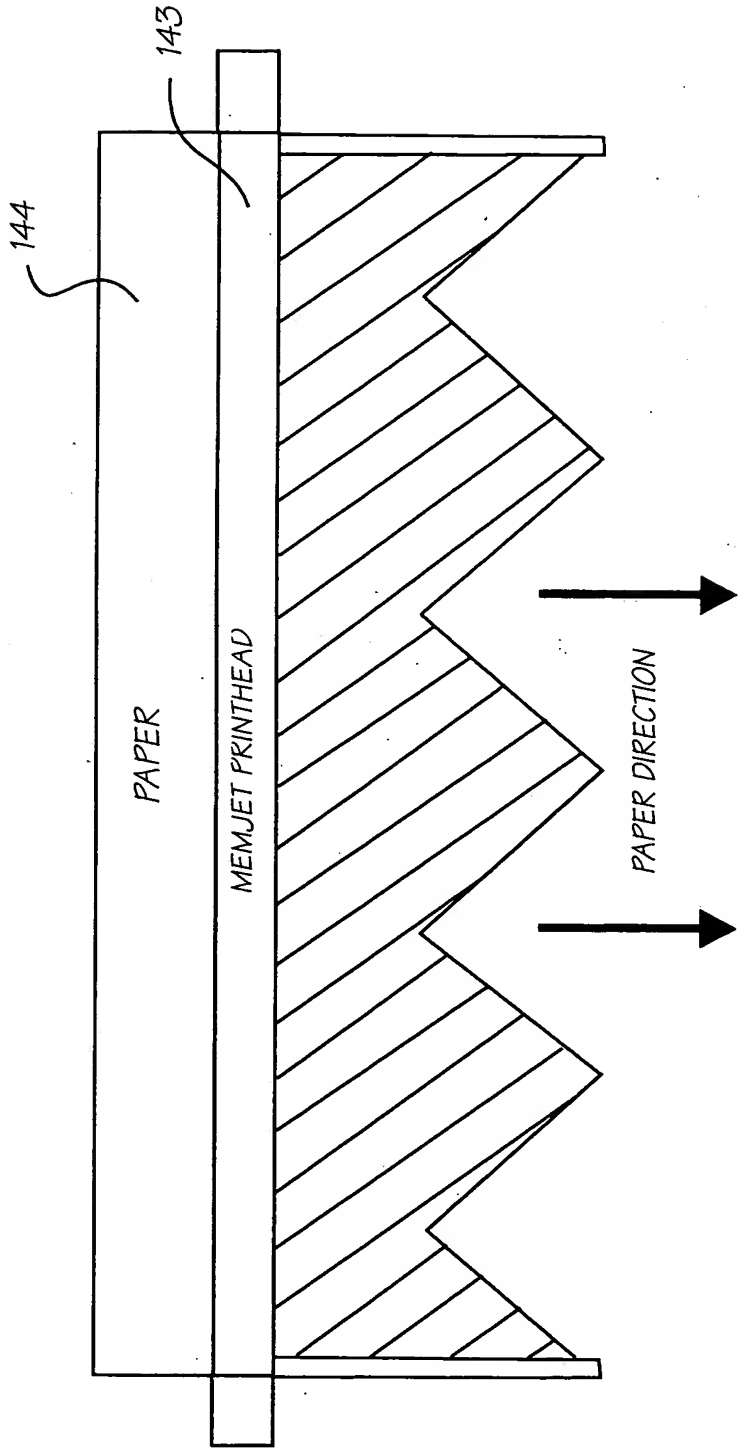


FIG. 31

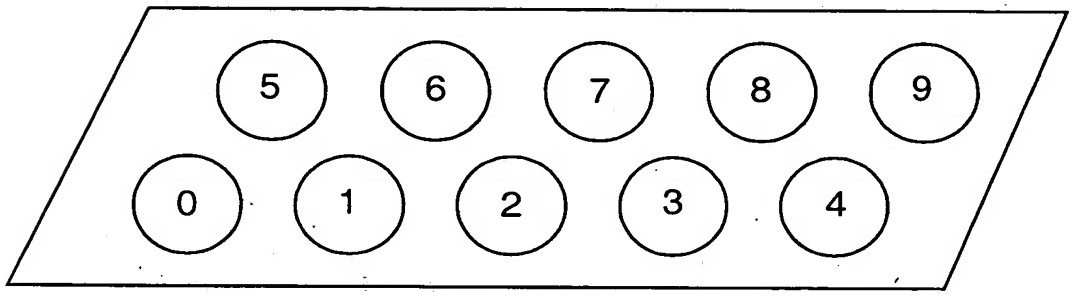


FIG. 32

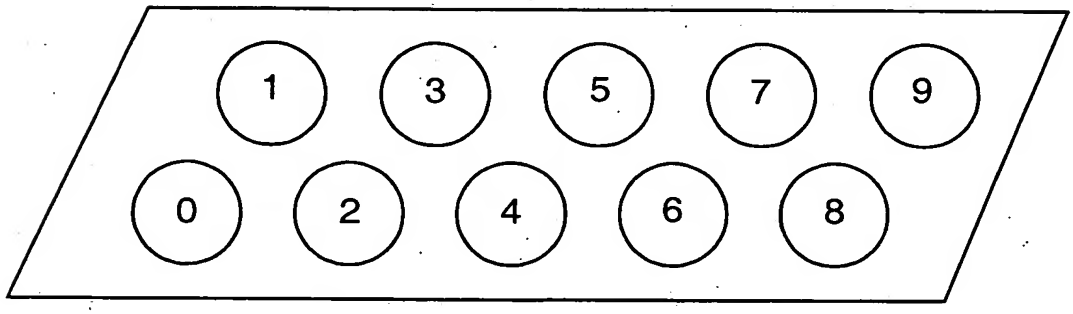


FIG. 33

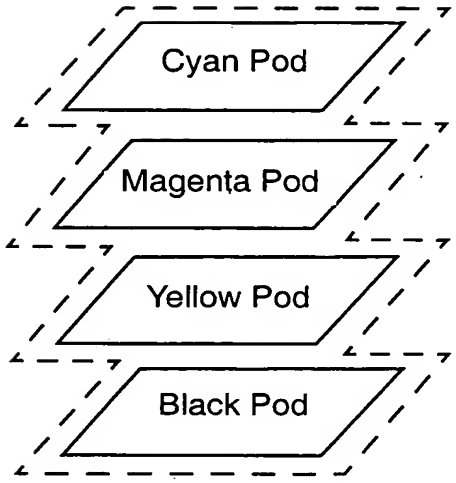


FIG. 34

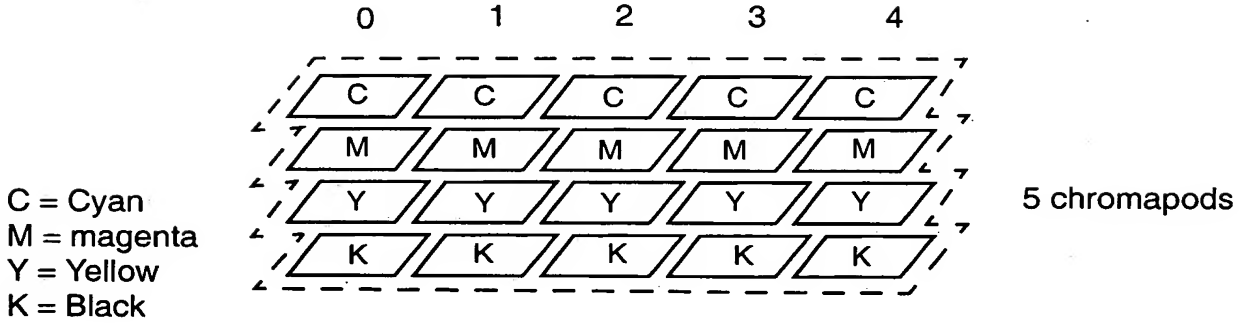


FIG. 35

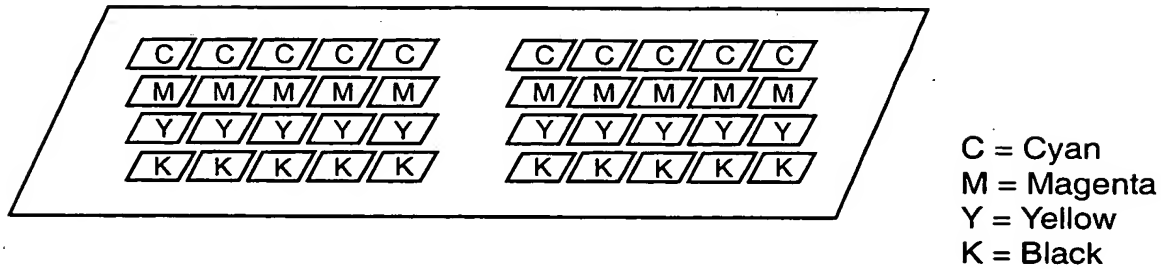


FIG. 36

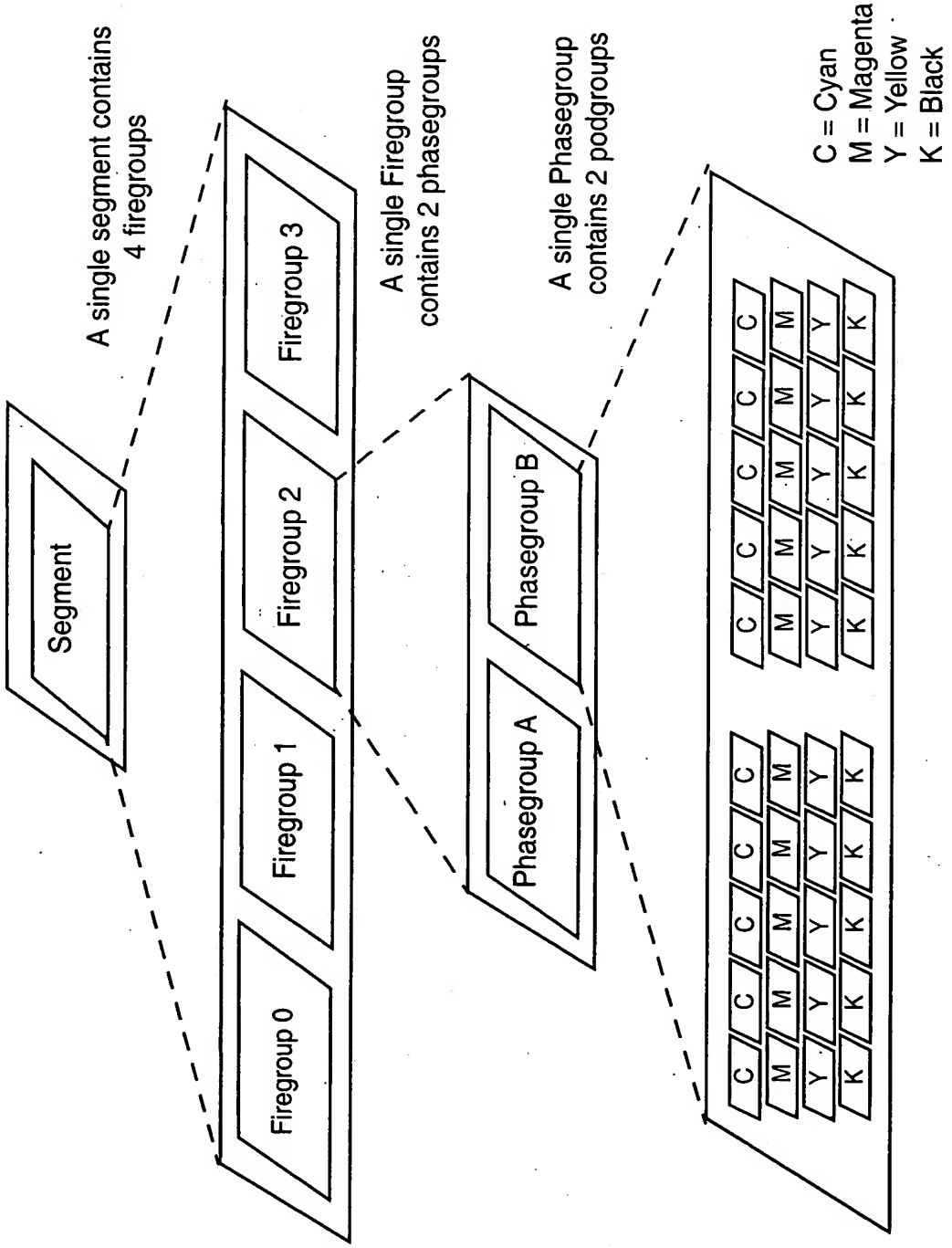

Segment
A single segment contains 4 firegroups
Firegroup 0
Firegroup 1
Firegroup 2
Firegroup 3
A single Firegroup contains 2 phasegroups
Phasegroup A
Phasegroup B
A single Phasegroup contains 2 podgroups
C = Cyan
M = Magenta
Y = Yellow
K = Black

FIG. 37

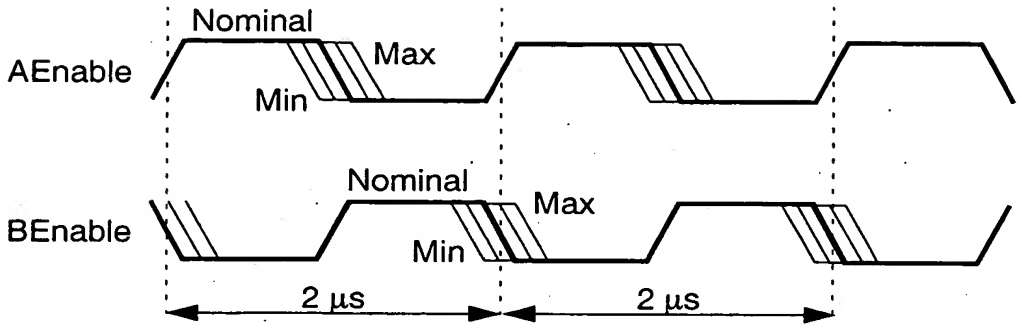

Nominal
Max
AEnable
Min
Nominal
Max
BEnable
Min
2 µs
2 µs

FIG. 38

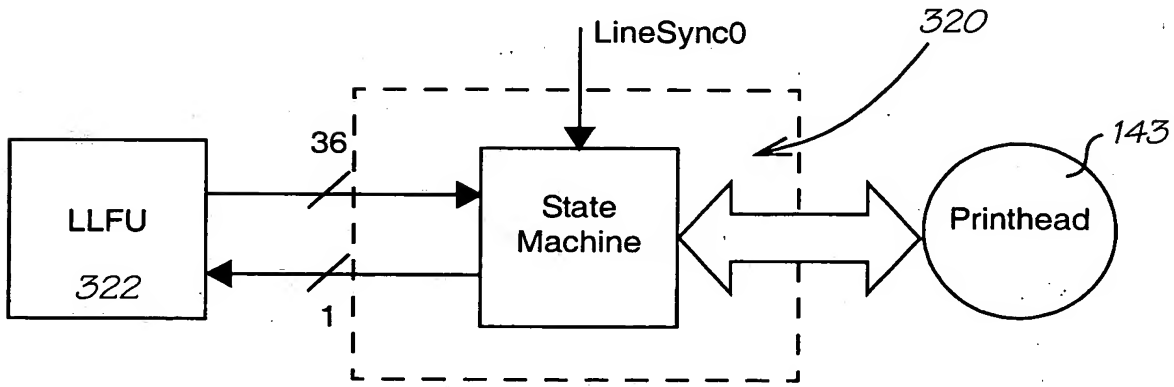

LineSync0
320
36
143
LLFU
322
State
Machine
Printhead
1

FIG. 40

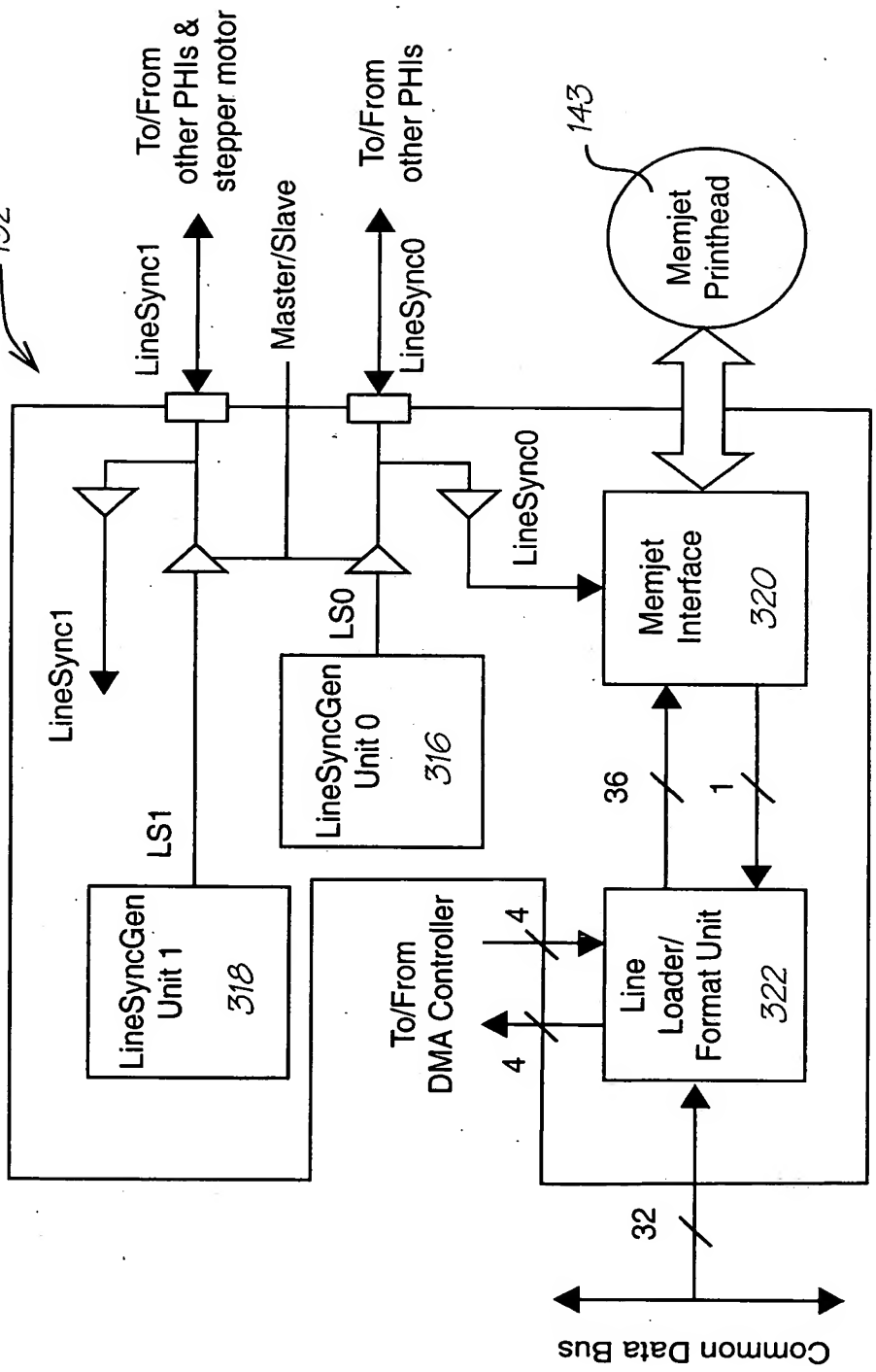

192
LineSync1
To/From other PHIs & stepper motor
Master/Slave
To/From other PHIs
LineSync0
143
Memjet Printhead
LineSync1
LS1
LineSyncGen Unit 1
318
LS0
LineSyncGen Unit 0
316
LineSync0
Memjet Interface
320
36
1
To/From DMA Controller
4
4
Line Loader/ Format Unit
322
32
Common Data Bus

FIG. 39

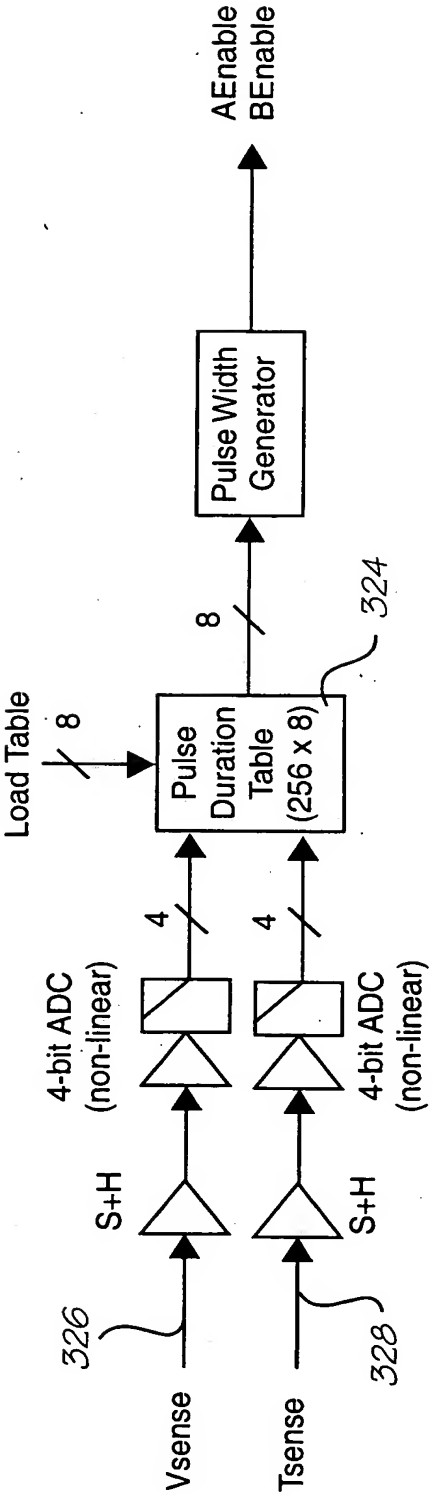

Vsense
Tsense
326
328
S+H
S+H
4-bit ADC (non-linear)
4-bit ADC (non-linear)
4
4
Load Table
8
Pulse Duration Table (256 x 8)
324
8
Pulse Width Generator
AEnable
BEnable

FIG. 41

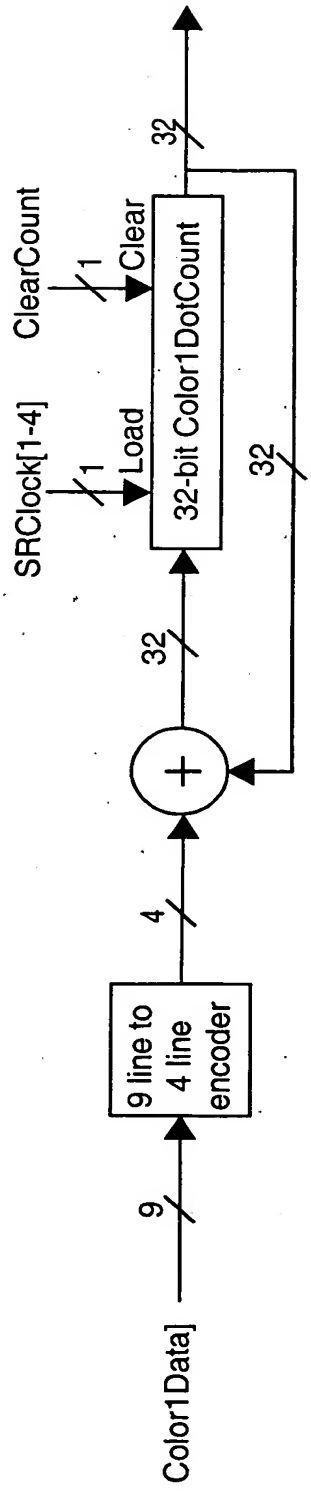

Color1Data]
9
9 line to 4 line encoder
4
32
SRClock[1-4]
1
Load
ClearCount
1
Clear
32-bit Color1DotCount
32
32

FIG. 42

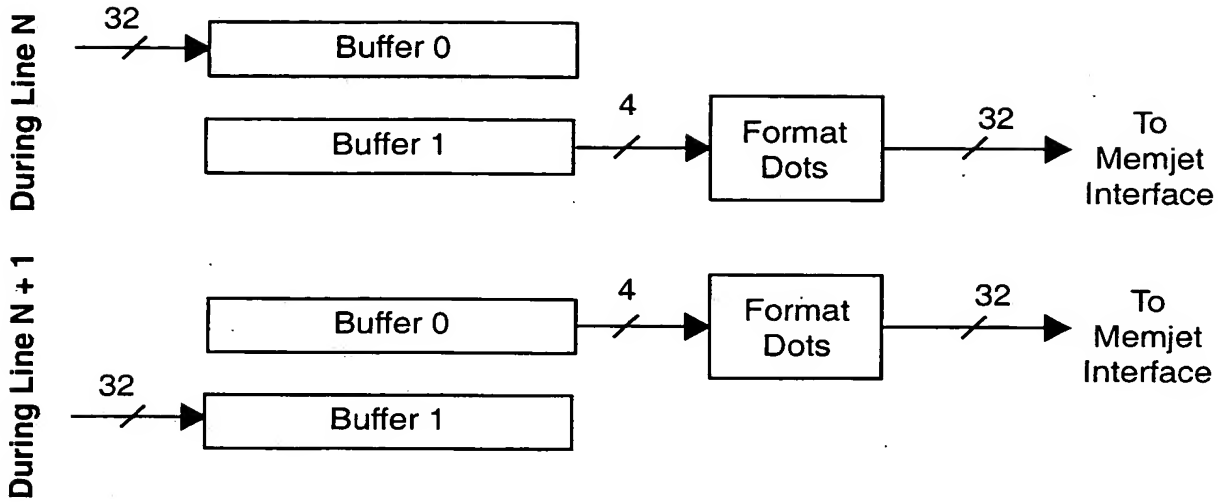

During Line N
32
Buffer 0
Buffer 1
4
Format Dots
32
To Memjet Interface
During Line N + 1
Buffer 0
4
Format Dots
32
To Memjet Interface
32
Buffer 1

FIG. 43

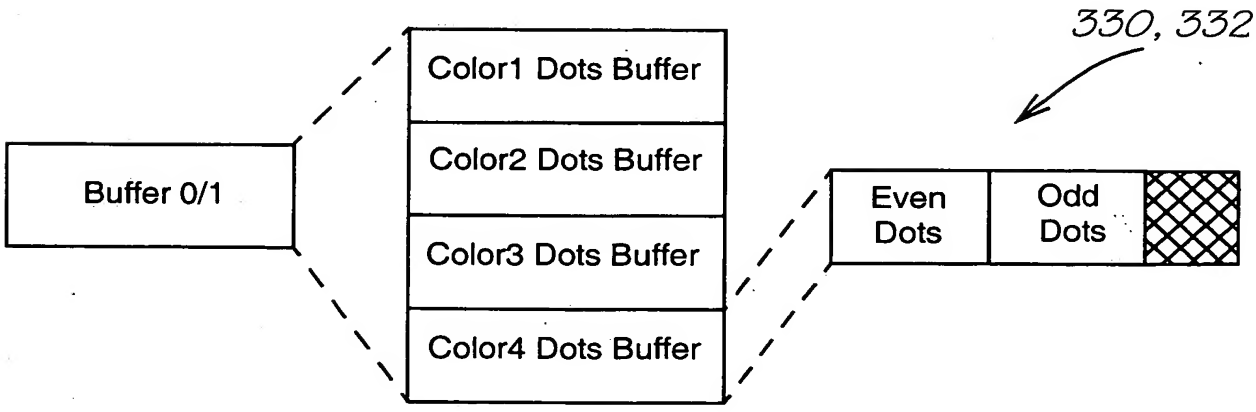

330, 332
Buffer 0/1
Color1 Dots Buffer
Color2 Dots Buffer
Color3 Dots Buffer
Color4 Dots Buffer
Even Dots
Odd Dots

FIG. 45

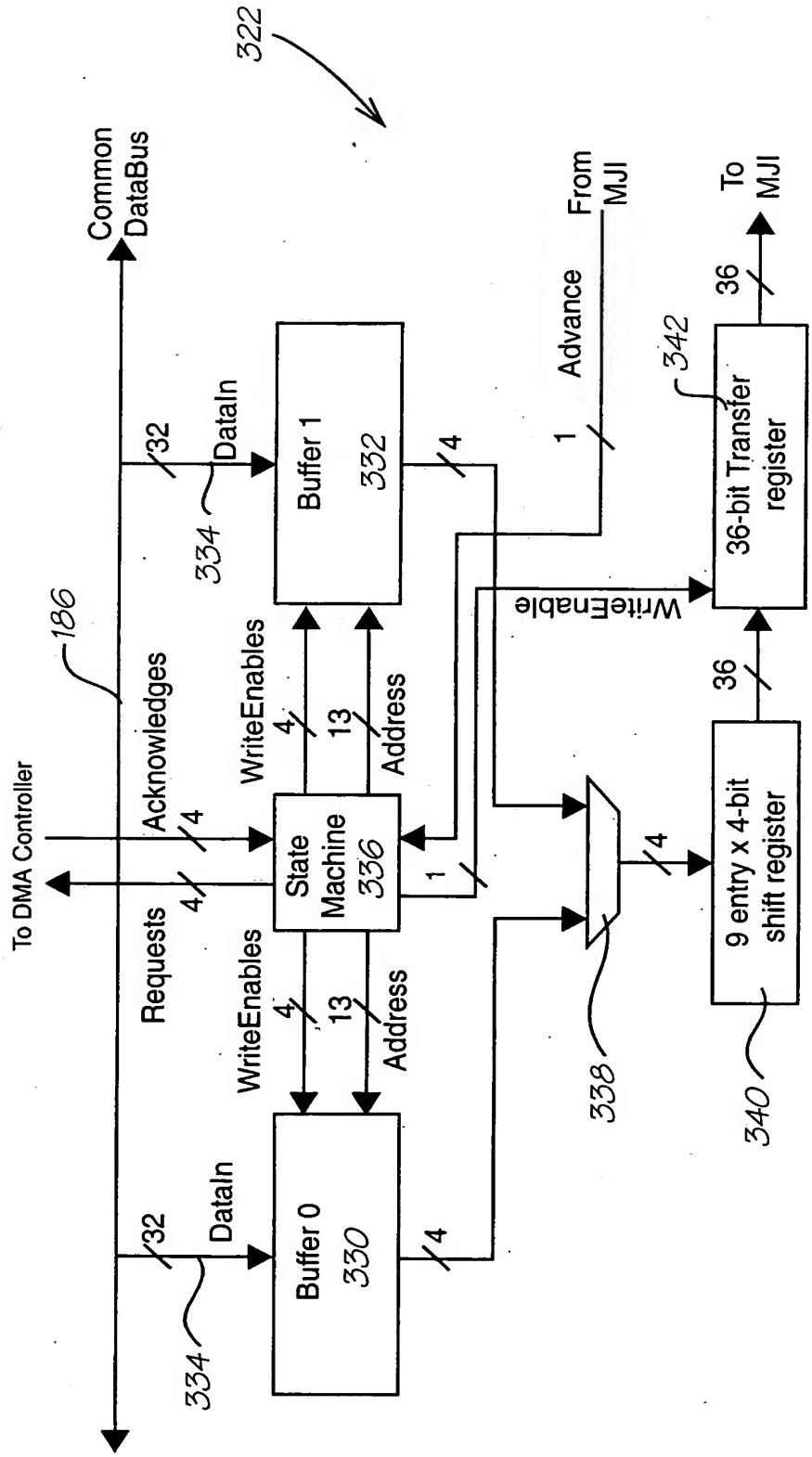

322
Common DataBus
186
To DMA Controller
Acknowledges
Requests
WriteEnables
Address
DataIn
Buffer 0
330
Buffer 1
332
State Machine
336
334
338
340
342
Advance
From MJI
WriteEnable
9 entry x 4-bit shift register
36-bit Transfer register
To MJI
32
4
13
1
36

FIG. 44

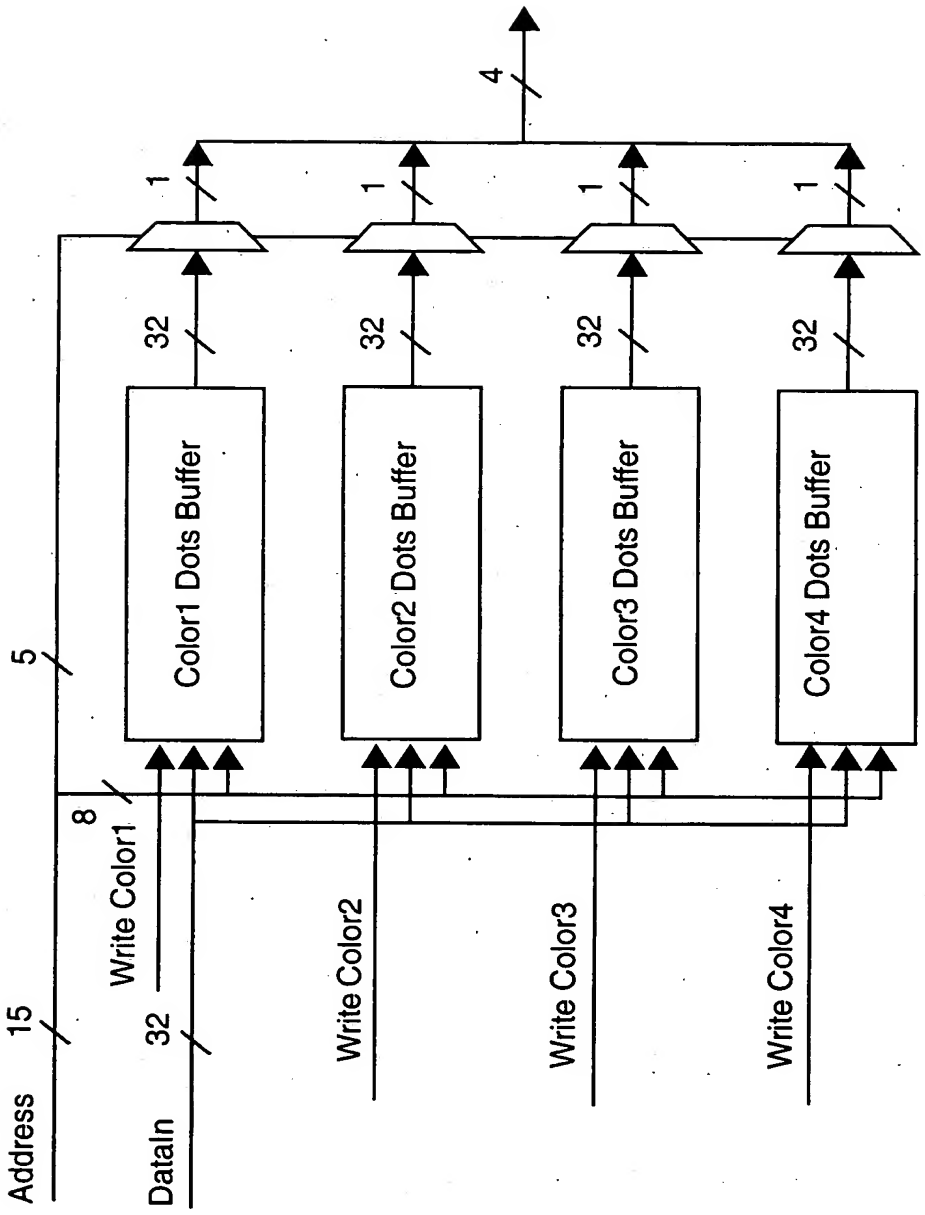

Address
15
DataIn
32
Write Color1
8
Write Color2
Write Color3
Write Color4
5
Color1 Dots Buffer
Color2 Dots Buffer
Color3 Dots Buffer
Color4 Dots Buffer
32
32
32
32
1
1
1
1
4

FIG. 46

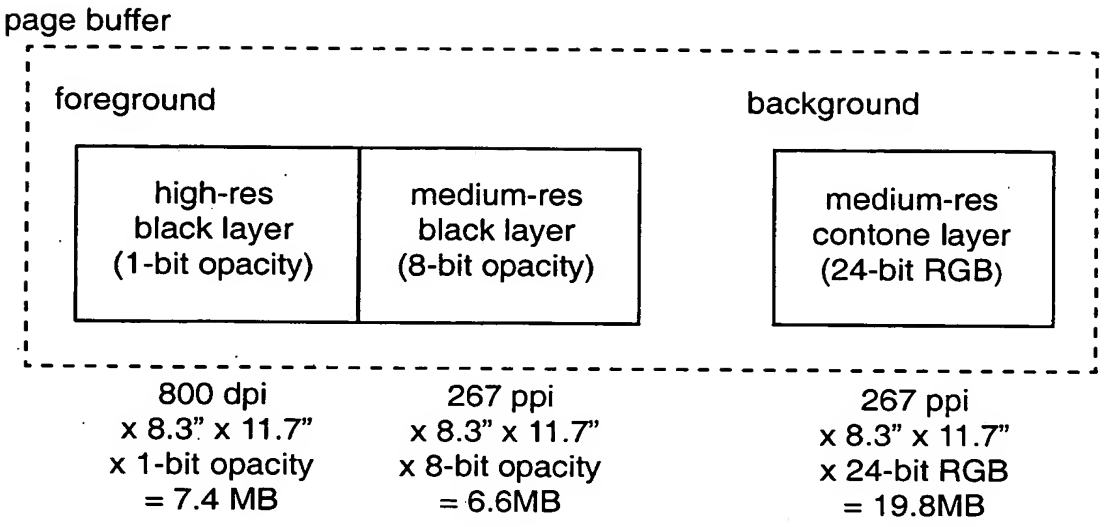

page buffer
foreground
background
high-res
black layer
(1-bit opacity)
medium-res
black layer
(8-bit opacity)
medium-res
contone layer
(24-bit RGB)
800 dpi
x 8.3" x 11.7"
x 1-bit opacity
= 7.4 MB
267 ppi
x 8.3" x 11.7"
x 8-bit opacity
= 6.6MB
267 ppi
x 8.3" x 11.7"
x 24-bit RGB
= 19.8MB

FIG. 47

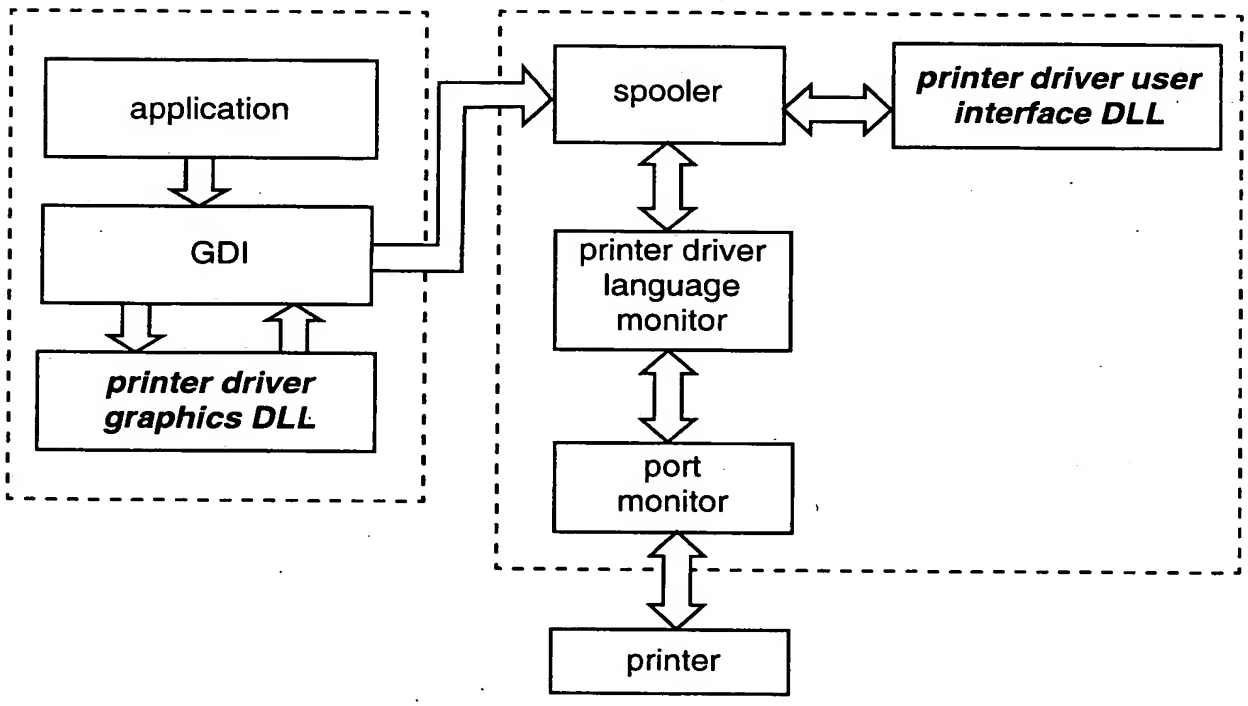

application
GDI
printer driver
graphics DLL
spooler
printer driver user
interface DLL
printer driver
language
monitor
port
monitor
printer

FIG. 48